Integrated DC Link Capacitor/Bus Structures to Minimize External ESL Contribution to Voltage Overshoot

M.A. Brubaker, H. C. Kirbie, and T. A. Hosking
SBE, Inc.,81 Parker Road, Barre, Vermont 05641
Info@SBElectronics.com

Abstract- Voltage overshoot is defined by stray series inductance and turn-off time, which must be managed to avoid failure of IGBT's in inverter applications. The total equivalent series inductance (ESL) is dictated by internal switch branch inductance with a significant contribution in the current path to the DC link capacitor. Using traditional topologies, external ESL dominates and by-pass capacitors ("snubbers") are used to mitigate overshoot. Integrated capacitor/bus designs provide an external ESL comparable to internal values for commercial IGBT's. The minimized ESL regime allows reduced switch turn-off time with slightly increased losses to manage overshoot without the cost, space, weight, dissipation, and reliability associated with by-pass capacitors.

I. INTRODUCTION

The SBE Power Ring Film Capacitor™ provides an optimal annular form factor with minimal Ohmic losses and excellent heat transfer capability. Utilizing a properly designed symmetrical terminal arrangement, a capacitor inductance on the order of 3 nH can be achieved for a 1000 µF capacitor rated at 600 V. When this capacitor structure is integrated with a suitable laminar bus topology for connection into the IGBT module, a significant reduction in equivalent series inductance (ESL) can be achieved as compared to traditional designs.

Operating in this new low-ESL regime, the need for external by-pass capacitors (often referred to as "snubbers") to mitigate voltage overshoot can potentially be eliminated by controlling the switch turn-off time. This strategy will help encourage widespread consumer adoption of electric vehicles by attacking inverter cost, weight, and size. While the reduction in turn-off time comes at a penalty of increased losses in the switch, the added heat load will be minimal and can be readily managed by the cooling hardware that is already present at the IGBT. In contrast, the losses for external by-pass capacitors can be significant, and these parts are more difficult to thermally couple to available cooling.

This paper presents calculated inductance data for an optimized annular form factor capacitor and terminal configuration. The simulation values have been validated using a ring-out test method to measure ESL and results are presented for relevant integrated capacitor/bus topologies. Having defined a new locus for minimized external ESL, circuit simulations were undertaken to explore possibilities for controlling voltage overshoot with gate control rather than external by-pass capacitors.

II. CALCULATION OF CAPACITOR INDUCTANCE

Consider the SBE 700D348 ring capacitor shown in Fig 1a which provides 1000 µF at 600 V. This part is constructed from a single monolithic winding of metallized polypropylene (MPP) film and fitted with two sets of concentric terminals. The capacitor was evaluated using the magneto-dynamic module in the Flux3D™ software package [1] with a 20 kHz sine wave having a magnitude of one volt at zero degrees phase applied across the terminals. Assuming a balanced voltage, the capacitor can be represented in 1/16 symmetry to significantly reduce the analysis domain size. The finite element analysis geometry and corresponding mesh is illustrated in Fig. 1b. Note that second order rectangular "brick" elements have been utilized to accurately treat the current distribution in the copper terminals where the skin depth is on the same order as the thickness.

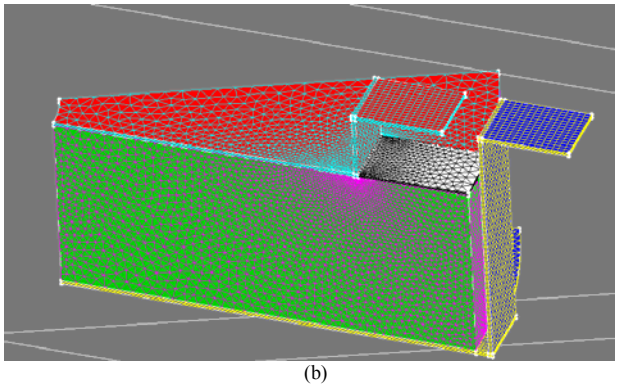
The current density in the capacitor terminals is influenced by both skin effect and mutual inductance as shown in Fig. 2. For an analysis plane cutting through both the inner and outer feet, current crowding (yellow) and heating occurs at the terminal edges. By integrating the normal current density across the capacitor cross section, the total current can be computed, from which the complex impedance is determined based on the known drive voltage. The resistive component of the impedance is then unfolded from the total power losses in the terminals and capacitor winding. The resulting inductance is 50.72 nH for the 1/16 symmetry geometry, which corresponds to a total inductance of 3.17 nH for the 1000 µF capacitor shown in Fig. 1.

III. ESL MEASUREMENTS

A. Method

The annular form factor capacitor is really a spatially-distributed impedance which can be very challenging to

(a)



(b)

Fig. 1. Illustration of finite element analysis domain for a 1000 µF annular form factor capacitor: a) actual capacitor, b) reduced domain using 1/16 symmetry showing mesh.

measure using a typical RLC bridge, particularly at higher frequencies. Recognizing the importance of understanding ESL for inverter applications, SBE has developed a ring-out method described previously [2] to easily measure the inductance of a capacitor/bus structure. Applying this technique to the capacitor shown in Fig. 1 mounted on a laminar bus structure indicates a capacitor inductance of 3.2 nH, which agrees very well with the simulation result. This correlation provides a good validation of both the simulation and measurement methods.

B. Integrated Capacitor and Bus Results

SBE has recently introduced a series of adapter kits to interface common IGBT modules with standard DC link capacitors using a low-inductance laminar bus. These parts have been characterized for ESL along with more advanced "vertically integrated" inverter topologies to demonstrate ESL values in the 20 nH regime [3]. For example, consider the

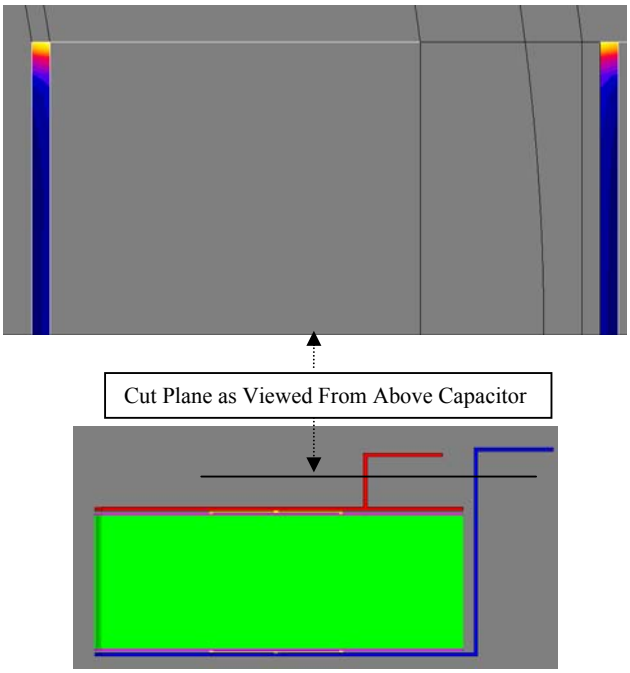


Fig. 2. Current density in capacitor terminals as viewed in a cut plane from above.

stacked topology, shown in Fig. 3 that represents a 100 kW system with a Danfoss E+ module, 500 µF DC link capacitor and laminar bus. The total ESL observed at the IGBT terminals for this case is 18.5 nH, which is significantly lower than typical reported values for conventonal DC link capacitors not including the interconnection [4].

A further improved capacitor and bus geometry is illustrated in Fig. 4. This is again a 100 kW vertical inverter configuration comprised of an Infineon HP2 switch module with two parallel 300 uF capacitors directly integrated to the laminar bus. Note that the capacitor orientation has now been rotated 180 degrees relative to Fig. 3 thus reducing the path length to the IGBT. Application of the ESL measurement technique to this structure indicates 15 nH at the IGBT terminals. Note that this value is on the same order as the

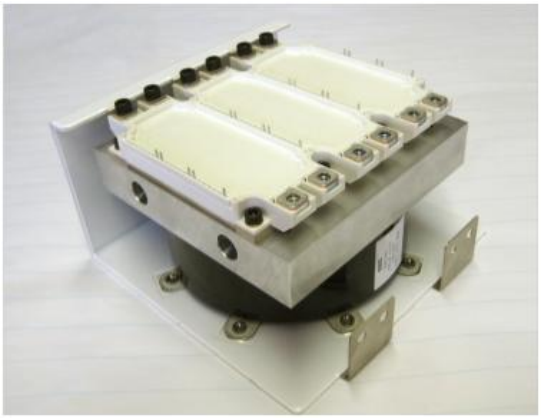


Fig. 3. Vertically integrated 100 kW inverter topology with an ESL of approximately 18.5 nH at the IGBT terminals.

Fig. 4. Vertically integrated 100 kW inverter with improved topology and a measured ESL of 15 nH.

internal package inductance for typical high power switch modules. The capacitor inductance is approximately 1.8 nH by virtue of paralleling the two windings, which is only 6% of the total loop ESL.

Voltage overshoot across the IGBT at turn off is defined by the total inductance in the loop comprised of the DC link capacitor, bus structure, and internal switch branches. The measurements presented here demonstrate that the external ESL contribution can be reduced to 15 nH, thus establishing a new low-ESL regime. The question remains as to how this breakthrough can be exploited for reduction of cost, weight, and volume in EV inverter applications. Elimination of traditional snubber capacitors will simultaneously address all three of these goals.

IV. Simulation of Overshoot for Low-ESL Regime

The dynamic interaction between the inverter's switching network and the distributed stray inductances can be examined with a simple network simulation. Fig. 5 illustrates a generic three-phase, voltage-source inverter connected to a common brushless DC motor. The network is powered by a battery and a bus-coupled, DC-link capacitor. The battery and DC link branches, inverter, and motor parameters are described in Tables 1, 2, and 3, respectively.

The tabulated values are placed in the simple network and modeled using Micro-Cap 10 [5]. Each switch is controlled using a sinusoidal pulse-width-modulation technique. One should note that the BLDC Motor model does not include a back emf, so the system has no load. Additionally, the gate control for the switching transitions is softened by an RC time so that snubber capacitors are not needed to reduce the simulation stiffness.

Table 1
Battery and DC link branch parameters.

Battery Branch		**DC-Link Branch**	
Voltage	325 V	Capacitance	500 µF
Series Resistance	10 mΩ	Cap. Series Inductance	3 nH
Cable Inductance	5 µH	Bus Inductance	12 nH

Table 2
Inverter parameters for the simulation.

IGBT Inverter					
Switches		**Gate Control**		**Operation**	
Inductance (nH each)	7	Gate RC Time (µs)	2.7	Modulation Freq. (kHz)	12.7
On-State (mΩ)	10	Control Transition:	Smooth	Power Freq. (Hz)	400
Off-State (MΩ)	100			Modulation Index	0.9

Table 3
Motor parameters for the simulation.

BLDC Motor			
Maximum Ratings		**Per Phase**	
Max RPM	10,000	Inductance	175 µH
Peak Power	55 kW	Resistance	10 mΩ @ 150 °C
Max Battery Voltage	450 V	Stator Winding	Sinusoidal
Max Phase Current	400 A	No. of Poles	12

One outcome of the Ideal Inverter simulation is the motor phase currents shown in Fig. 6. The A-phase period is 2.5 ms (400 Hz) with a peak current of about 330 A (233 A RMS). A great deal more information is available in the simulation, including all control functions, switching states, and component voltages and currents.

In order to just examine the worst-case voltage overshoot

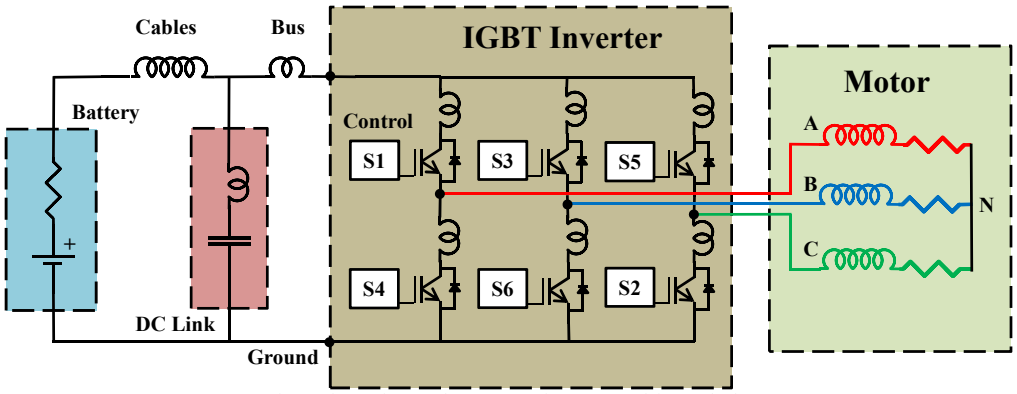


Fig 5. Three-phase voltage source inverter used for analysis.

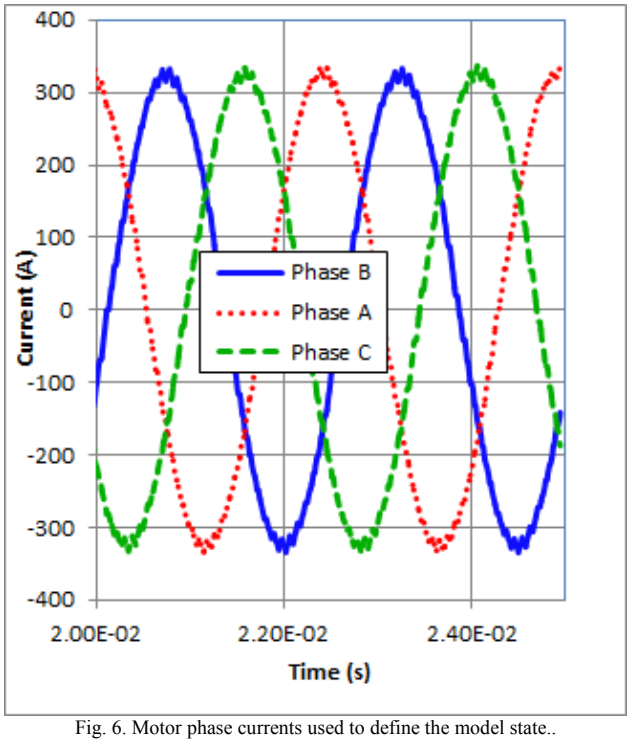


Fig. 6. Motor phase currents used to define the model state..

of a single switch opening, we used the Ideal Inverter simulation to set the network's state variables at a moment when the A-phase branch has reached a peak current and is about to toggle between S4 and S1. That moment occurs at 26.183 ms into the simulation run. The Simplified Inverter network, shown below in Fig. 7, incorporates the Ideal Inverter's state variables plus an IGBT model in place of ideal switches.

The red and green boxes are switch macro-models containing four IGBT networks in parallel, as shown in Fig. 8. The networks are Hefner [6] representations of an IXYS High-Current IGBT, IXSX80N60B, which is a 600-V, 160-A component and available in the Micro-Cap 10 library. The macro-model diode is assigned a forward impedance of 2 mΩ.

The red boxes represent switches that are closed in positions S4, S6, and S5, with switch S4 about to open when the control pulse, V6, goes from high to low. Green boxes represent switches that are open in positions S1, S3, and S2 and remain open throughout the simulation. The state variables from the Ideal Inverter simulation are shown in the circuit diagram as initial conditions (IC=X). Positive currents are directed into the positive (+) end of the inductor. The capacitor voltage of 320.16 V is slightly less than the battery value of 325 V. Inductors that have no initial conditions are assigned zero-current values because the state currents from the Ideal Inverter simulation were very small. On-state values of the gate drive (DC or pulsed) are 20 V.

Having explained the methodology, the results of the Simplified Inverter simulation are now presented. One should note that initial conditions could not be established within the IGBT macro-switch models. Consequently, the simulation must run a few microseconds until steady-state conditions are reached and S4 can be opened. The steady-state inductor currents and those prescribed by the Ideal Inverter simulation differ by less than 10 A in any circuit branch when S4 opens.

The voltage across S4 after opening is presented in Fig. 9, which also shows the voltage across each component in the loop comprised of L10, L1, L7, L8 and C1. Note that the voltage across the DC link in Fig. 9 does not include the capacitor voltage, which remains at a DC value of 317.4 V during the opening. As expected, the switch voltage is defined by Kirchoff's law as the summation of the voltages around the loop. Defining the inductance values shown in Fig. 7 as Case 1, the effect of changing the various inductances in the switch loop can now be evaluated.

Three additional cases were defined for comparison. Case 2 represents a very optimistic scenerio where all of the loop inductances are reduced to a value of 1 nH. Case 3 is the same as Case 2, except that both of the branch inductances for the switches have been restored to 7 nH. Finally, Case 4 was constructed using 7 nH for the switch branches, with conventional values of 30 nH for the DC link capacitor and 120 nH for the interconnection to the IGBT. The voltage

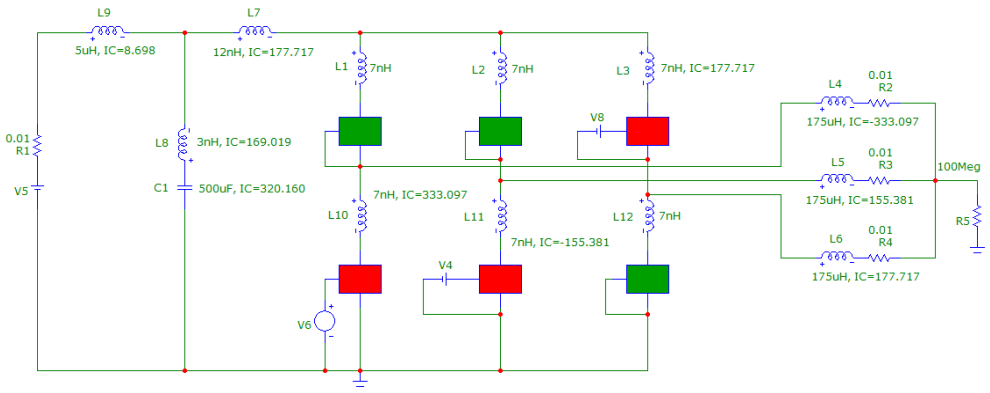


Fig. 7. Simplified analysis circuit with state variables as initial conditions (Case 1).

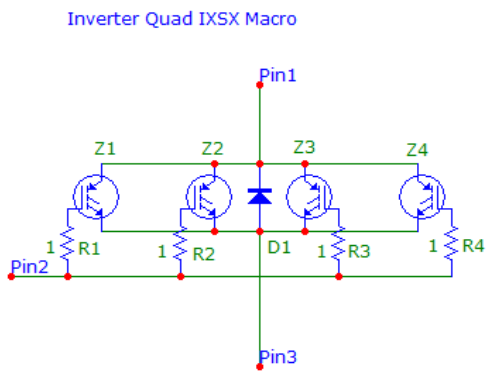


Fig. 8.Illustration of the equivalent circuit used to model the IGBT's.

overshoot across S4 after opening is compared for each of the four cases in Fig. 10.

The overshoot behavior offers some very interesting insight into the relative contributions of the various inductances. As might be expected, a much more severe overshoot condition is observed for the worst case with a conventional DC link capacitor and traditional interconnection having a relatively large ESL. Similarly, the low-ESL regime enabled by the integrated bus and capacitor structures shown earlier in the paper clearly reduces the voltage peak. However, the further reduction of external ESL beyond the levels achieved here has minimal impact given the IGBT branch inductance. In effect, switch packaging issues that have been traditionally masked by the DC link capacitor and bus are now in the spotlight.

One should note that the overshoot response for Case 4 is not sinusoidal because the IGBT macro-model begins to

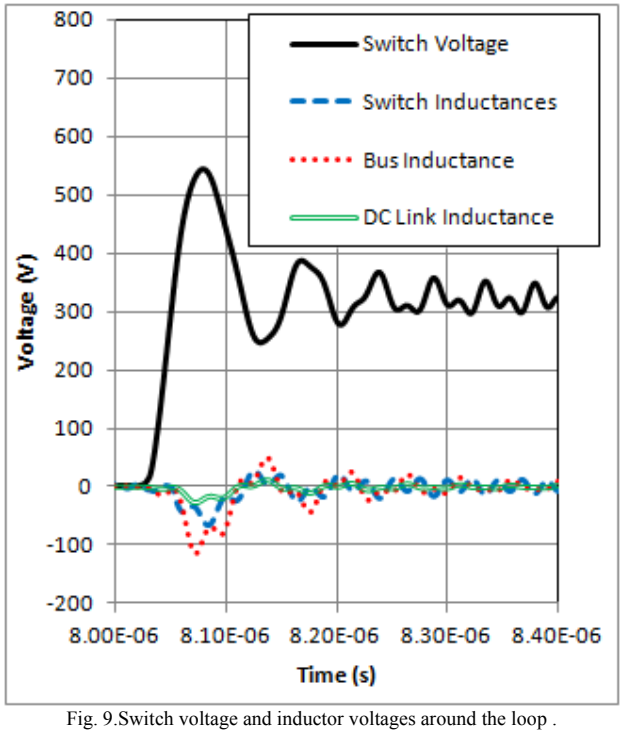


Fig. 9.Switch voltage and inductor voltages around the loop .

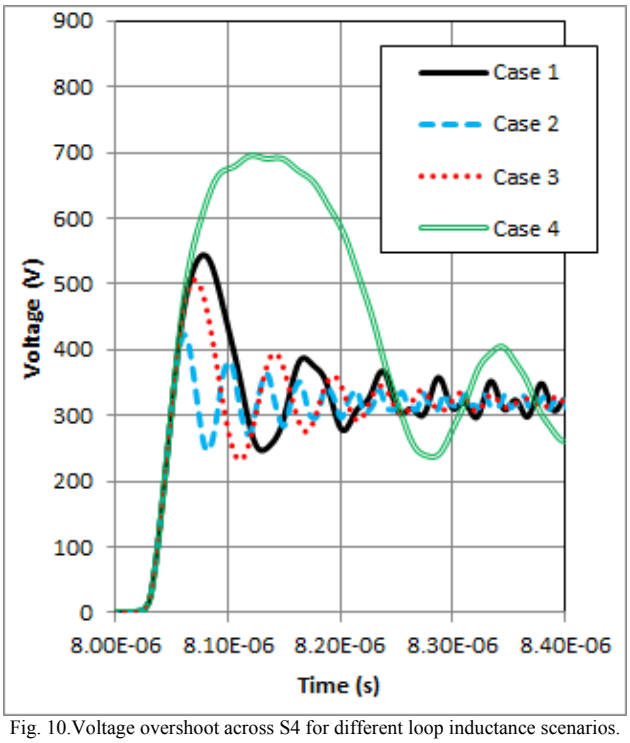


Fig. 10.Voltage overshoot across S4 for different loop inductance scenarios.

Case 1: L_{cap} = 3 nH, L_{bus} =12 nH, L_{switch} = 7 nH

Case 2: L_{cap} = 1 nH, L_{bus} =1 nH, L_{switch} = 1 nH

Case 3: L_{cap} = 1 nH, L_{bus} =1 nH, L_{switch} = 7 nH

Case 4: L_{cap} = 30 nH, L_{bus} =120 nH, L_{switch} = 7 nH

exhibit a rapidly growing nonlinear behavior for collector voltages greater than 600 V. With the gate voltage maintained at zero, the model transitions into a high-current breakdown knee at 1.33 kV.

V. Discussion and Conclusions

The new low-ESL regime, achieved by an integrated bus and SBE Power Ring Film Capacitor™, establishes the DC-link and bus inductance on the same order as a typical IGBT switch-package inductance. That low-ESL condition is the best it can be (see Fig. 10 Case 1) without blurring the boundaries between capacitor, bus and switching. Further reduction of ESL will now require effort directed at the switch packaging and terminal configurations. Simulations indicate that the low-ESL inverter still produces overshoot without snubbers, but the amplitude is now manageable by less snubbing and/or advanced gate control.

The path of advanced gate control [7] offers the ability to exploit the low external ESL to eliminate snubber assemblies and gain a significant savings in cost and space. The tradeoff is in IGBT heating produced by a managed slower turn-off time versus heating produced by snubber stored energy at turn-on. Additionally, the Ohmic heating of the snubber capacitors must be acknowledged as part of the discussion. The low-ESL regime makes the managed gate turn-off

approach more attractive by less stored energy in the network's stray inductance. Furthermore, optimized gate control offers IGBT protection against inverter short circuits without snubbers. Additional work is clearly required to understand the system level optimization required to best exploit the new low-inductance regime.

ACKNOWLEDGMENTS

The authors wish to thank Mr. Michael Stibgen at Methode Electronics for his help with the design and fabrication of the bus structures utilized for testing. We also appreciate contributions from Mark Bellinger at Infineon and Siegbert Haumann at Danfoss on IGBT module interfaces.

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