Integrated DC link capacitor/bus enables a 20% increase in inverter efficiency

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The Power Point presentation will be available after the conference.

Abstract

Voltage overshoot at switch turn-off traditionally limits the DC operating voltage for inverter systems. Mitigation methods include snubber capacitors and intelligent gate control, which add cost and complexity while reducing efficiency. However, the fundamental first step in overshoot reduction is actually minimizing the DC link inductance. The combination of the SBE Power Ring Film Capacitor™ integrated with an optimized bus structure can achieve a DC link inductance below 10nH (approaching 5nH), which is less than typical IGBT half-bridge internal branch values. This enables safely increasing the DC voltage up to 20% as compared to standard configurations, thus improving inverter performance and volume efficiency with existing IGBT's.

1. Introduction

Voltage overshoot occurs during IGBT turn-off due to energy stored in the stray inductance applied across the die. It is typical to operate at a DC voltage well below the IGBT limit to avoid catastrophic failure, which reduces the inverter power. Snubber capacitors can be added to mitigate overshoot to some degree, but this approach adds cost, requires additional cooling and has the potential for creating unwanted resonances. Using intelligent gate control to slow down the turn-off transition is another option, but this increases the switching losses. Overshoot management must ultimately be addressed at the system level, but minimizing the stray inductance is clearly the critical first step to increasing the amount of useable power for a given investment in IGBT's.

Inductance contributions are provided by the DC link capacitor, bus structure and internal IGBT branches. Conventional DC link capacitors have relatively large equivalent series inductance (ESL) values [1] and designers traditionally consider this the largest contributor to voltage overshoot. However, recent advances in capacitor form factor and terminal optimization have dramatically altered the situation and capacitors with an ESL of less than 5nH have been demonstrated [2]. With this development, the DC link bus and particularly the interconnect structure to the IGBT has become the limiting factor [3].

This paper provides analysis and testing of different IGBT input configurations and compares "through-hole" and "tabbed" input styles. Overshoot testing results are correlated with previously presented "ring-out" measurements [2]. Testing of an optimized single phase prototype capacitor/bus topology demonstrates that the external contribution to ESL can actually be reduced to less than the IGBT branch inductance of a half-bridge. This substantial reduction of voltage overshoot translates into a 20% increase in DC operating voltage, and a corresponding improvement in inverter power using the same IGBT's.

2. Analysis

Overshoot is determined by the stray inductance looking back into the DC link from the IGBT die, which has contributions from the capacitor, bus bar, and internal connections of the IGBT module. The interconnection between the bus structure and the IGBT terminals has a surprisingly large effect and the Flux3D [4] magneto-dynamic finite element analysis platform has been used to evaluate the inductance of relevant half-bridge IGBT input configurations. A laminar bus bar with a 0.5mm spacing between the plates was selected as the basis for comparison. A "tab" style scenario was defined based on the input geometry of a typical 1400A discrete half-bridge module with a respective

tab length and width of 25.4mm and 18mm. The tabs were spaced by 37mm, which defines the effective loop area at the input connection.

Copper was assumed for the bus material and driving potentials were applied to establish the required current flow at a harmonic frequency of 10kHz. The net impedance was unfolded based on the total current flow through the conductor cross sections and the resistive component was calculated from the total losses computed in each conductor. Based on these results, the reactive component of the impedance was established from which the inductance was determined to be 12.8nH. The current density distribution for the "tab" style input is presented in Figure 1(a), which shows how the current concentrates at the inside edges of the tabs.

A more symmetrical "through-hole" style of connection can be implemented to provide a more favorable current distribution with reduced inductance. The key to this approach is to fill in as much of the loop area as possible with copper while maintaining a safe creepage distance between the conductors. The computations were performed in the same manner described for the tab geometry and the current density distribution is presented in Figure 1(b). The inductance for this case was found to be only 4nH, which is more than a factor of three better than the tab geometry. Analysis of additional frequencies down to 2.5kHz was undertaken for both geometries to confirm that the ESL values did not change appreciably. Based on the analysis results, the through-hole approach was selected for the optimized capacitor/bus prototype design.

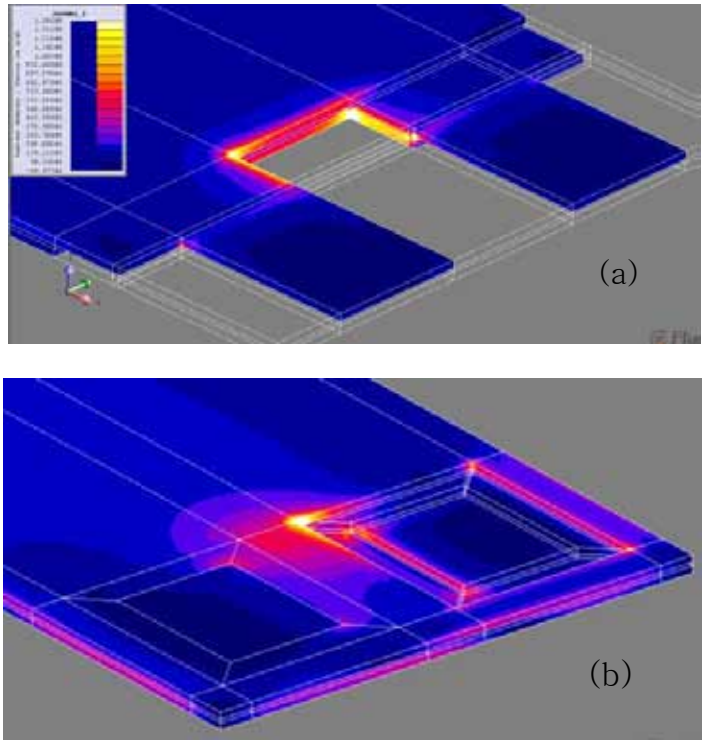


Figure 1(a) and (b): Comparison of current density distributions for tab and through-hole inputs.

3. Optimized Prototype Design

Based on the analysis results in the previous section, an optimized single phase capacitor/bus prototype was developed through collaboration between SBE and Danfoss Silicon Power as shown in Figure 2.

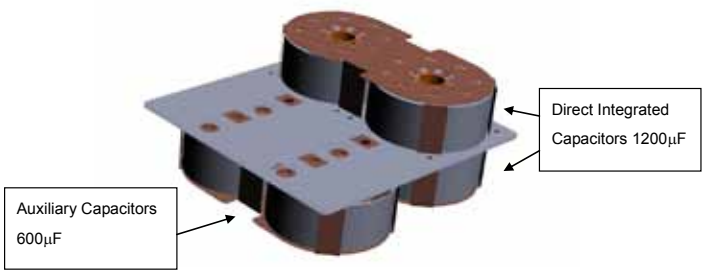


Figure 2: Optimized cap/bus single phase prototype for evaluation.

The capacitor "building block" is a 300μF Power Ring Film Capacitor™ deployed in a 2x2 back to back array on a laminar bus. The capacitors are directly integrated to the bus plates to eliminate redundant copper and "crown" terminals are incorporated to provide magnetic flux cancellation for low ESL. The "ring" form factor also minimizes both the ESR and thermal resistance of the windings such that doubling of the system power can be achieved without compromising life. Through-hole connections are provided for two half-bridge modules. Note that two additional auxiliary 300μF capacitors can be added after the IGBT's are installed if additional capacitance is required.

4. Inductance Versus Overshoot

The "ring-out" test method has been described previously [2] for characterizing DC link capacitor and bus bar inductance using a relatively simple test circuit. This approach has been validated by overshoot testing similar to the "double pulse" method [5] with the apparatus shown in Figure 3(a). An integrated sensing resistor provides an accurate measure of the turn-off current such that the inductance can be determined from the overshoot voltage. By measuring the overshoot voltage at the IGBT terminals, it is possible to determine the inductance contribution of the capacitor and bus. Using an SBE 700D525 capacitor (1000μF and 900V) with the arrangement shown in Figure 3(a), the overshoot voltage indicates a capacitor/bus inductance of 16.7nH. Note that this configuration has a tab geometry, so the inductance will be higher than with through-hole connections. Performing the ring-out test on the same geometry indicates an induc-

tance of 16.5nH which shows very good correlation.

The ring-out method was applied to the optimized single phase cap/bus prototype described in the previous section without the auxiliary capacitors. The inductances for each half-bridge input pair are shown in Figure 3(b). The adapter fixture required to connect the discharge switch for the ring-out test across the through-holes will add a bit of inductance, so we believe that the measured values of 6-8nH are a bit higher than the actual value. This has been confirmed by the testing undertaken at Danfoss Silicon Power as described in the next section.

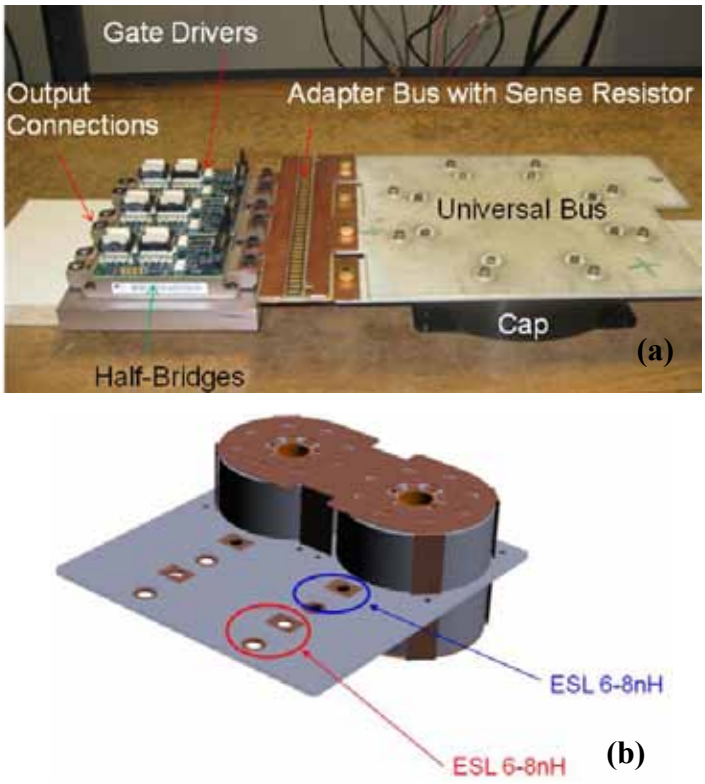


Figure 3: (a) Overshoot testing apparatus, (b) Measured inductances for an optimized capacitor and bus structure.

5. Testing at Danfoss Silicon Power

5.1 Experimental Results

To benchmark the optimized capacitor and bus bar structure it is compared to a bus bar from a Danfoss power stack that already has a very low stray inductance since it is equipped with foil capacitors. The test setup is shown in Figure 4 with two P3 power modules connected in parallel in the middle of the bus bars. The double pulse test is applied to measure overvoltage during turn-off and di/dt and ΔV during turn-on to calculate the stray inductance.

All measurements are taken with the lower transistor switching while the gate of the upper IGBT is kept in the off

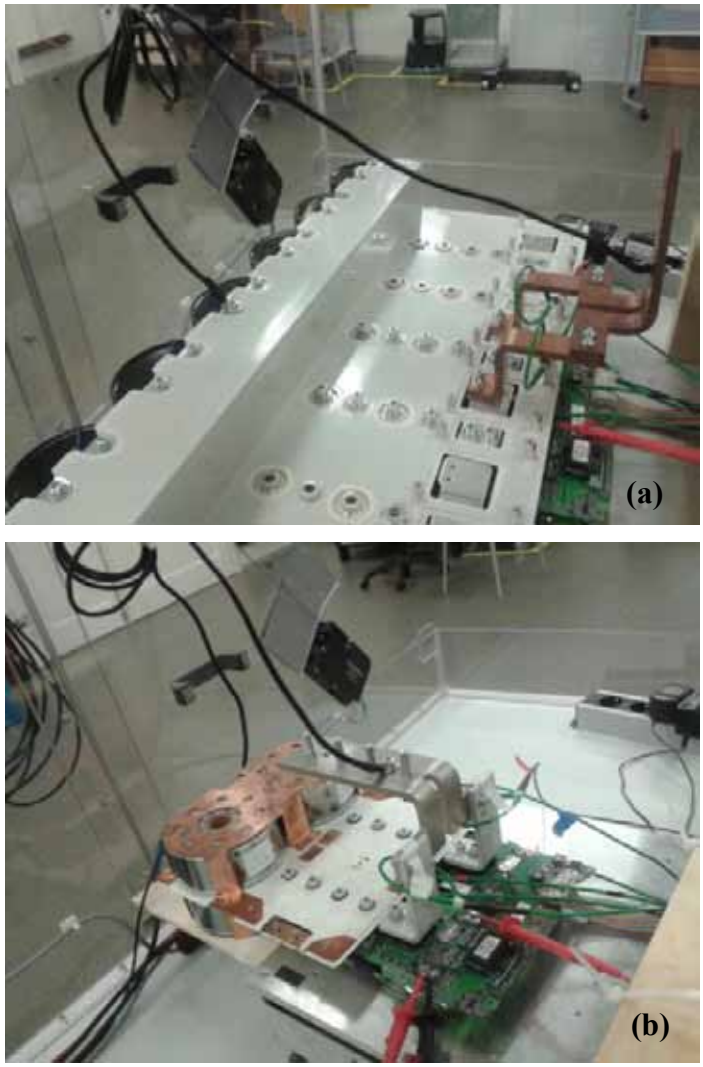


Figure 4: Bus bar with capacitors: (a) Danfoss, (b) SBE Power Ring Capacitors

condition ($_{V_{ge\_upper}}$= -10Vdc). Between the common output terminal of the modules (terminal 8) and positive bus bar, a 3.6uH choke (L_{load}) is connected. Base plate temperature of module under the test is 25C. Turn on resistor value is 0.5 Ohms and turn off resistor value is 1 Ohms for both lower IGBT. Voltage applied to bus bar is between 600Vdc and 1100Vdc. Figure 5 shows the schematics of the test setup and the probe placement. Rogowski Current Transducers are placed around module terminals 10 and 12, differential voltage probes are connected between terminals 1-2 and terminals 3-2. The stray inductance is calculated by measuring the current di/dt and the DC-link voltage dip at the AUX terminals at IGBT module at turn on. The voltage dip is a consequence of the di/dt through the series of stray inductances that are present at the bus bar and the components in the current paths.

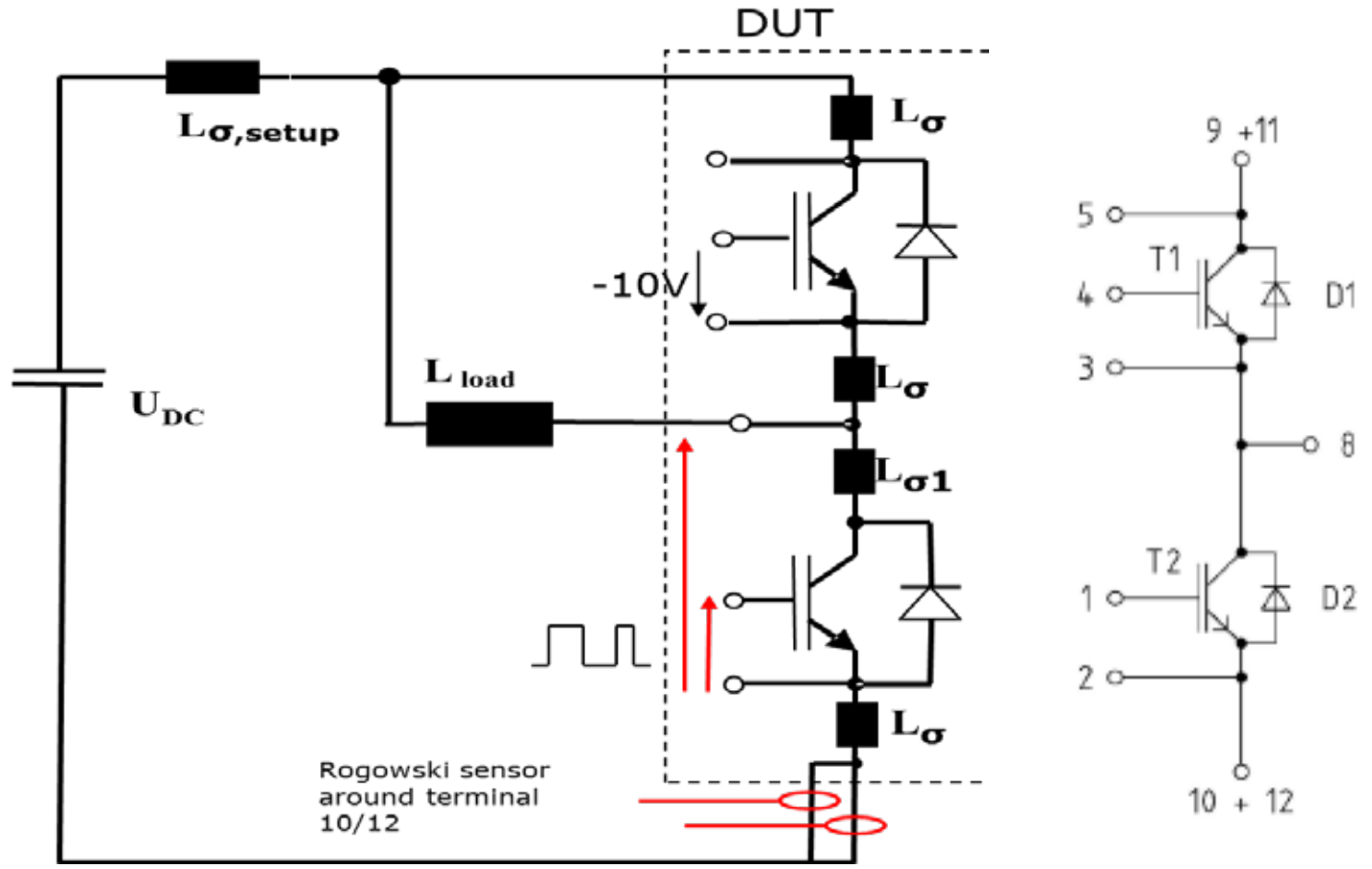


Figure 5: Schematic of the test setup and probe placement

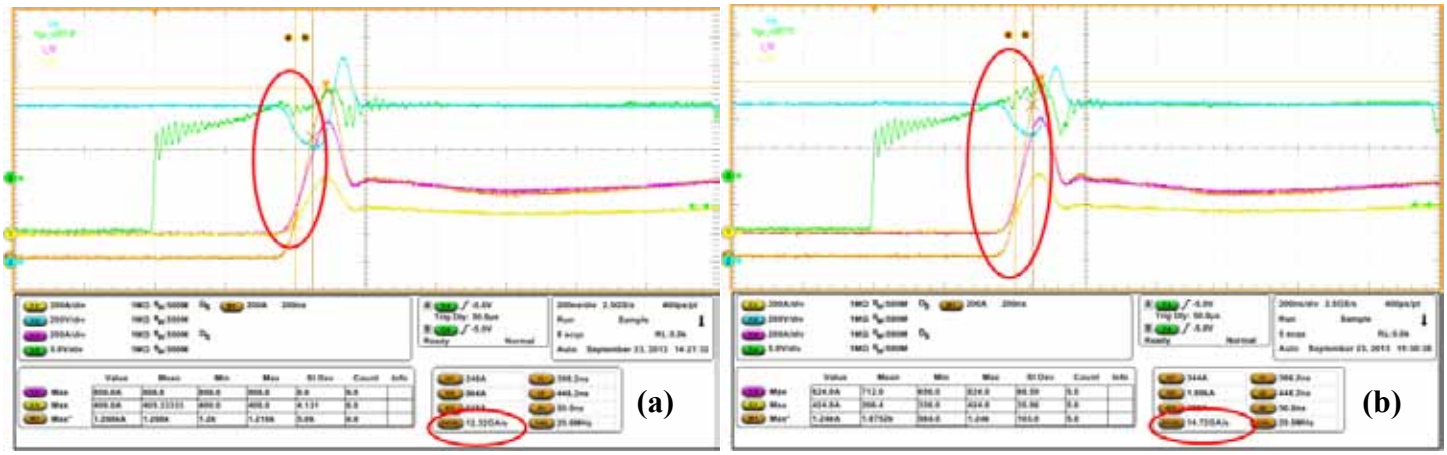


Figure 6: Waveforms for calculating stray inductance: (a) standard foil capacitor, (b) proposed SBE Power Ring Capacitors

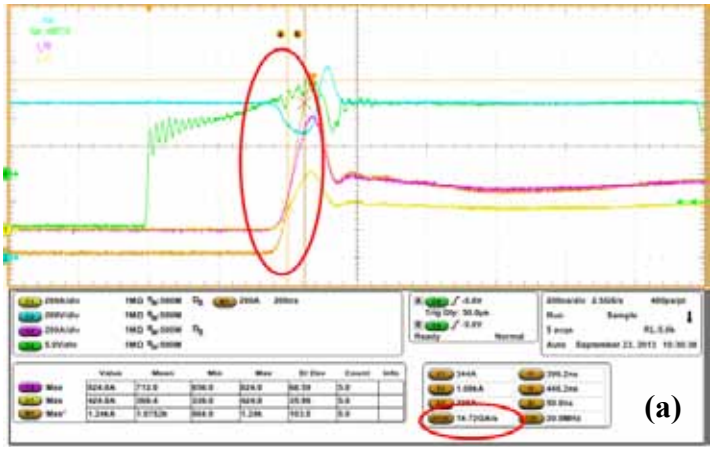
5.2 Stray inductance

The stray inductance for both setups is measured during turn on according to equation $L_s = \Delta V\ dI/dt$. The waveforms are shown in Figure 6. The description of signals is given in Table 1. The DC-link voltage is 1100 V and the peak current is measured to 1200 A.

Ch1 (yellow)	Ic term 12	Ch2 (blue)	Vce term 2-3
Ch3 (purple)	Ic term 10	Ch4 (green)	Vge term 2-1
M1 (brown)	M1 (brown)		

Table 1: Probes description

For the standard bus bar ΔV is 296 V and dI/dt is 12,3kA/µs, which leads to a stray inductance of 24nH for the whole current path including capacitors, bus bar and IGBT module. For the SBE setup ΔV is 224V and dI/dt is 14,7kA/µs resulting in a stray inductance of 15 nH for the whole current path. By measuring the voltage V_{ce} across the whole module (Ch2 V_{ce} term 9-10, AC-coupling) the stray inductance of the module is neglected as per Figure 7. With ΔV = 65V and di/dt = 14,7kA/µs the stray inductance of the bus bar and the capacitors is calculated to 4,4nH, while 10nH are expected to be inside the power module, that is consistent to the datasheet.



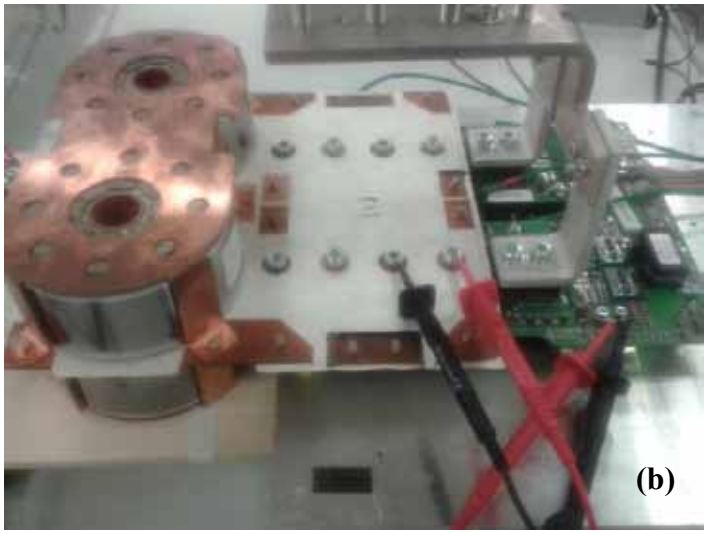
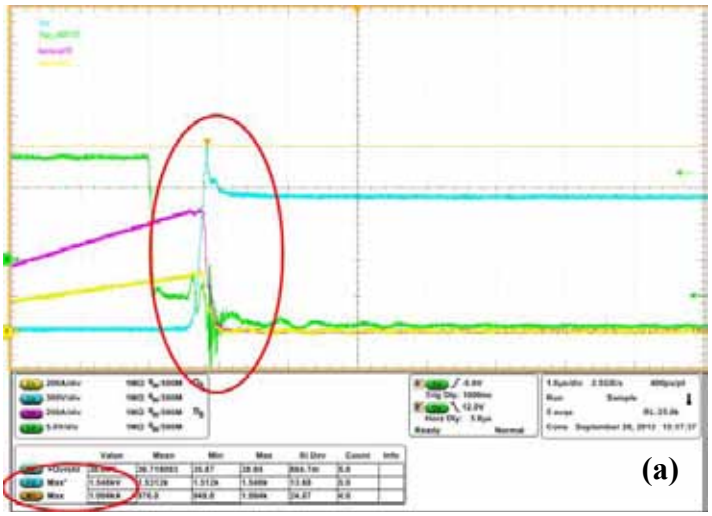


Figure 7: (a) Turn on waveform, neglecting the stray inductance of the module, (b) Measuring setup

5.3 Voltage Overshoot at turn off

To determine what effect the reduced stray inductances will have on the turn off voltage transient, a comparison is made between the setups as shown in Figure 8.



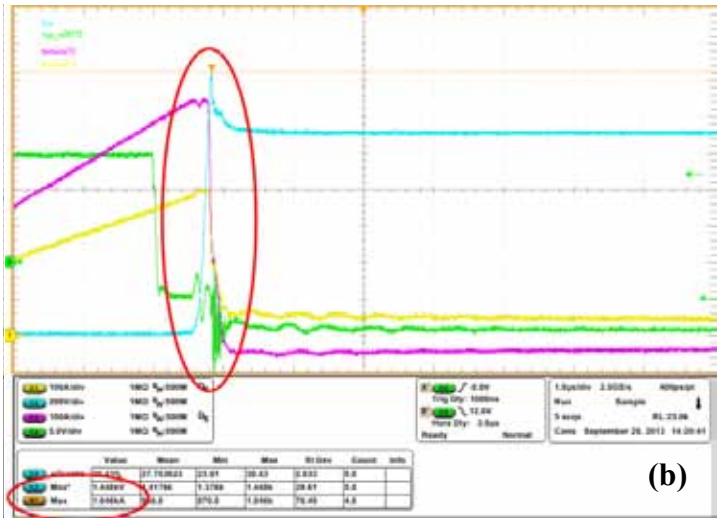


Figure 8: Waveforms for measuring the overshoot of the voltage during turn on: (a) standard foil capacitor, (b) proposed SBE Power Ring Capacitors

For the standard capacitors a voltage overshoot of 448V at 1000A could be detected while the overshoot for the SBE design is with 348V, which is 100V less at a slightly higher current of 1046A.

6. Conclusion

Voltage overshoot traditionally limits the DC operating voltage of high power inverters to a value significantly less than the IGBT limit. Reducing the inductance of the DC link capacitor and bus structure will reduce this overshoot and thus allow safely increasing the operating voltage to harvest more power using existing IGBT's. Magneto-dynamic analysis combined with ring-out and overshoot measurement has been used to develop an optimized DC link capacitor/bus configuration with minimal ESL. Independent testing has demonstrated that this design has achieved an unprecedented cap/bus inductance of < 5nH.

The single phase prototype demonstration unit shown in Figure 2 was constructed using four 300µF ring capacitors deployed back to back on a laminar bus to achieve a 1200µF DC link. Through-hole connections to the IGBT's combined with crown terminal connections to the capacitors were utilized to minimize the total ESL seen at the switches. Danfoss Silicon Power has performed testing on the prototype and measured an ESL contribution of 4.4nH for the capacitor/bus. This is less than half of the 10nH inductance expected for the half-bridge IGBT branches. The corresponding reduction in overshoot voltage is more than 20% which means that the DC bus voltage can safely be increased by the same amount. As such, a 20% increase in inverter power can be readily achieved with the same investment in silicon, which is a clear win in the highly competitive alternative energy market space.

7. References

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