Integrated DC link capacitor/bus enables a 20% increase in inverter efficiency

PCIM 2014

M. A. Brubaker, D. El Hage, T. A. Hosking, E. D. Sawyer - (SBE Inc. – Vermont, USA)
Toke Franke Wolf - (Danfoss Silicon Power – Flensburg, Germany)

SBE Inc. Booth 9-140
Danfoss Silicon Power Booth 9-360

Overview

- Introduction
- Analysis of IGBT input configuration
- Optimized prototype design
  - SBE’s overshoot & ring out measurements
  - Testing at Danfoss Silicon Power
- Further work - Full scale “power stack” module
- Conclusions
- Questions

Introduction (1)

- Inverter performance highly dependent of stray inductance value generating voltage overshoot at each turn-off cycle:
  - Snubbers -> added cost and complexity
  - Intelligent gate control -> slow down turn-off transition -> added switching losses

- Ultimate solution is minimizing the total stray inductance -> increased operating voltage and power by 20% - *Invested Semiconductor Efficiency*

Introduction (2)

- Inductance contributions :
  - DC link capacitor,
  - Bus structure,
  - Internal IGBT branches.
- Different IGBT input configurations will be evaluated
- Inductance and overshoot measurements will be conducted -> validate 20% overshoot reduction with SBE’s integrated capacitor/bus

Analysis of IGBT input (1)

- Flux3D magneto-dynamic finite element analysis platform used to evaluate the inductance of relevant half-bridge IGBT input configurations.

- A laminar bus bar with 0.5mm spacing between copper plates selected as the basis for comparison.

- Harmonic frequency of 10 kHz

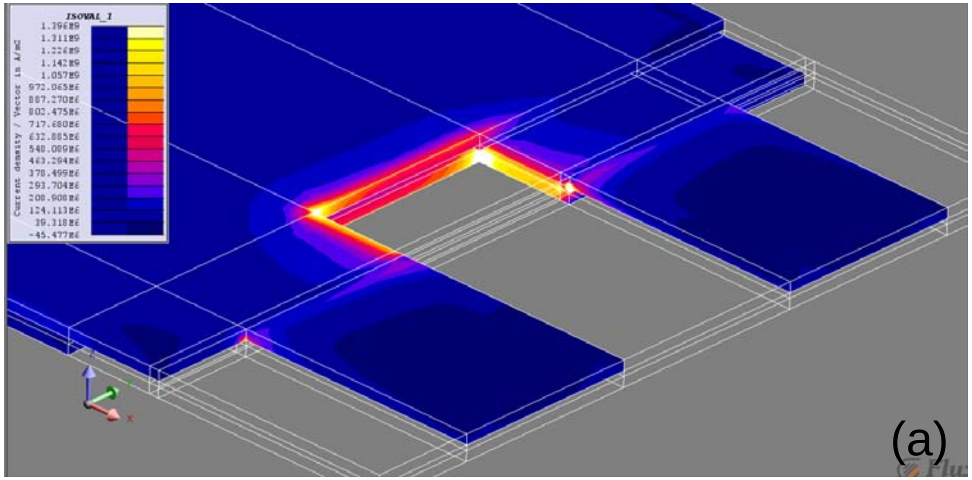
Analysis of IGBT input (2)

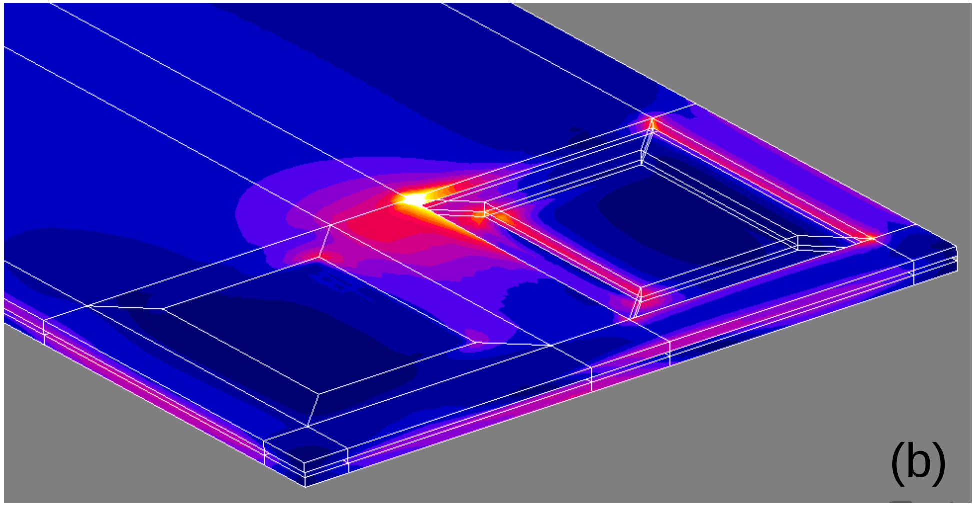
1. *Net impedance unfolded based on the total current flow through conductor cross sections and driving potential,*
2. *Resistive component calculated from total losses in each conductor,*

Reactive component impedance established using above calculations - Inductance simulated:

12.8 nH for a "tab style" connection
Only 4 nH for a "through hole" connection

Analysis of IGBT input (3)

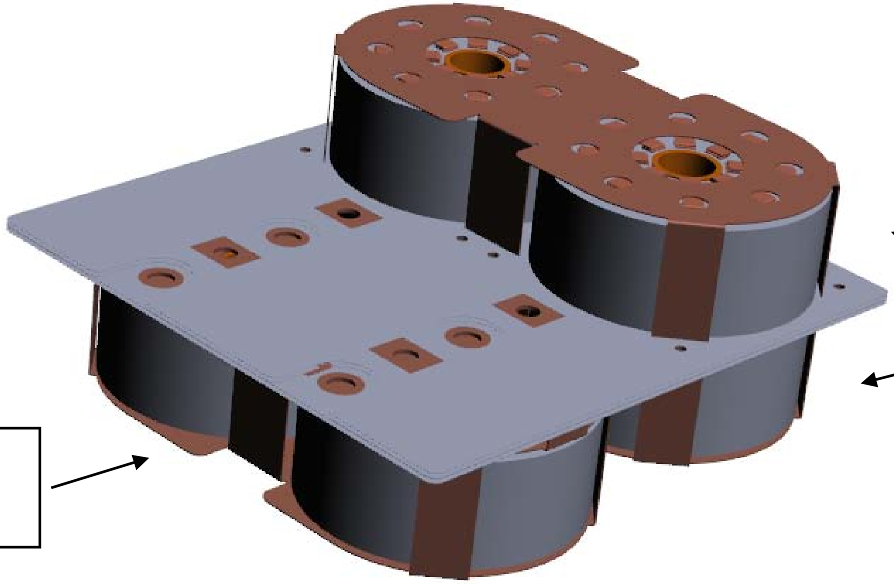




- Comparison of current density distribution for “tab” (a) and “through-hole” (b) inputs.
- Input geometry of a typical 1400A discrete half-bridge module -> defines loop area at input connection.

Optimized prototype design (1)

Optimized single phase capacitor/bus prototype developed through collaboration between SBE & Danfoss Silicon Power



Direct Integrated Capacitors 1200μF

Auxiliary Capacitors 600μF

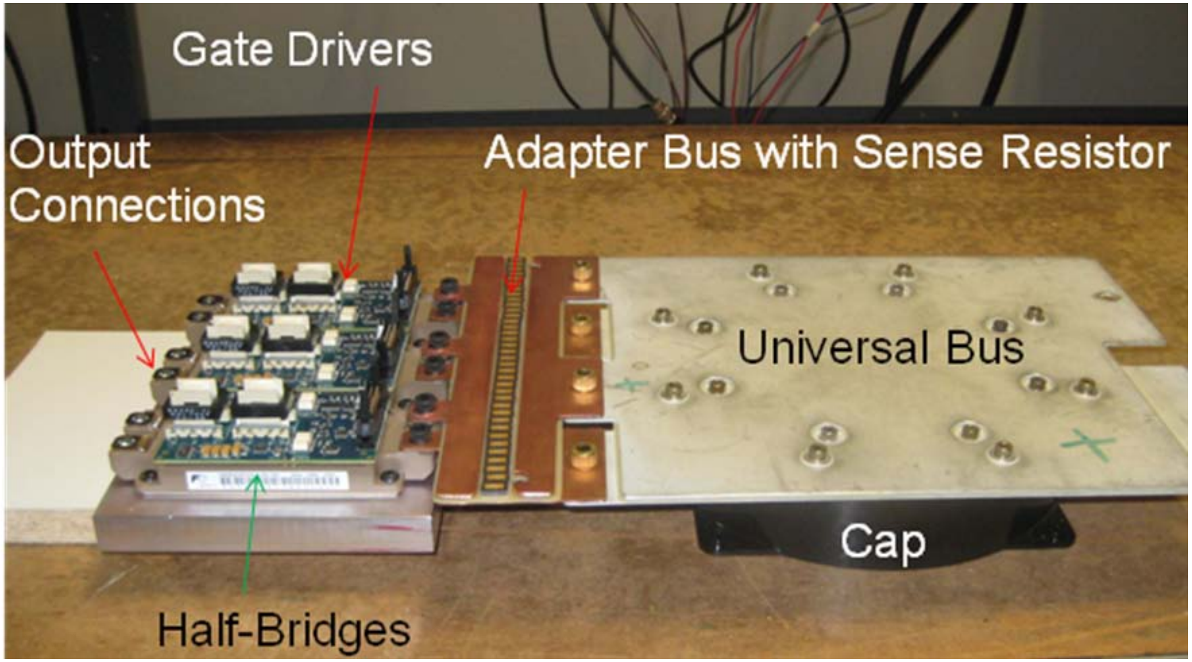
Optimized prototype design (2)

- Capacitors directly integrated to the bus plates -> less copper & better magnetic flux cancellation for low ESL,
- “Ring” form factor also minimizes ESR and thermal resistance of the windings,
- “Through-hole” connections for two half-bridge modules,
- Two auxiliary 300µF capacitors - if additional capacitance is required.

SBE’s measurements (1)

- Overshoot testing setup:
  - ✓ *Integrated sensing resistor for accurate measurement of turn-off current,*
  - ✓ *Overshoot voltage measured at the IGBT terminals will determine inductance contribution of the capacitor and bus,*
- SBE’s “ring out” test method correlates with overshoot testing -> Validated by measuring customized & standard parts – results also correlate with customer testing and simulations.

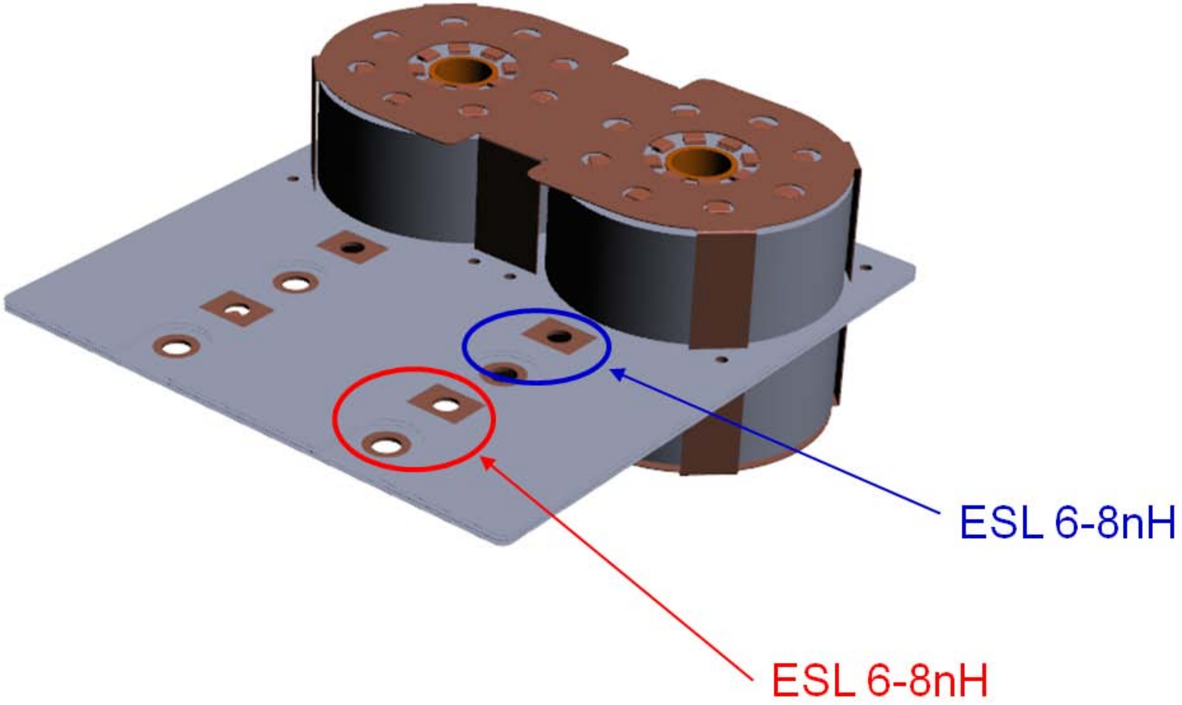
SBE’s measurements (2)



SBE overshoot testing apparatus – used also to validate “ring out” test [*] measurements

[*] E. D. Sawyer, “Low Inductance - Low Temp Rise DC Bus Capacitor Properties Enabling the Optimization of High Power Inverters”, Proceedings of PCIM, Nuremberg, Germany, May 2010

SBE's measurements (3)



Measured inductances for the optimized capacitor and bus structure using "ring out" test method.

Testing at Danfoss Silicon Power (1)

Comparison:

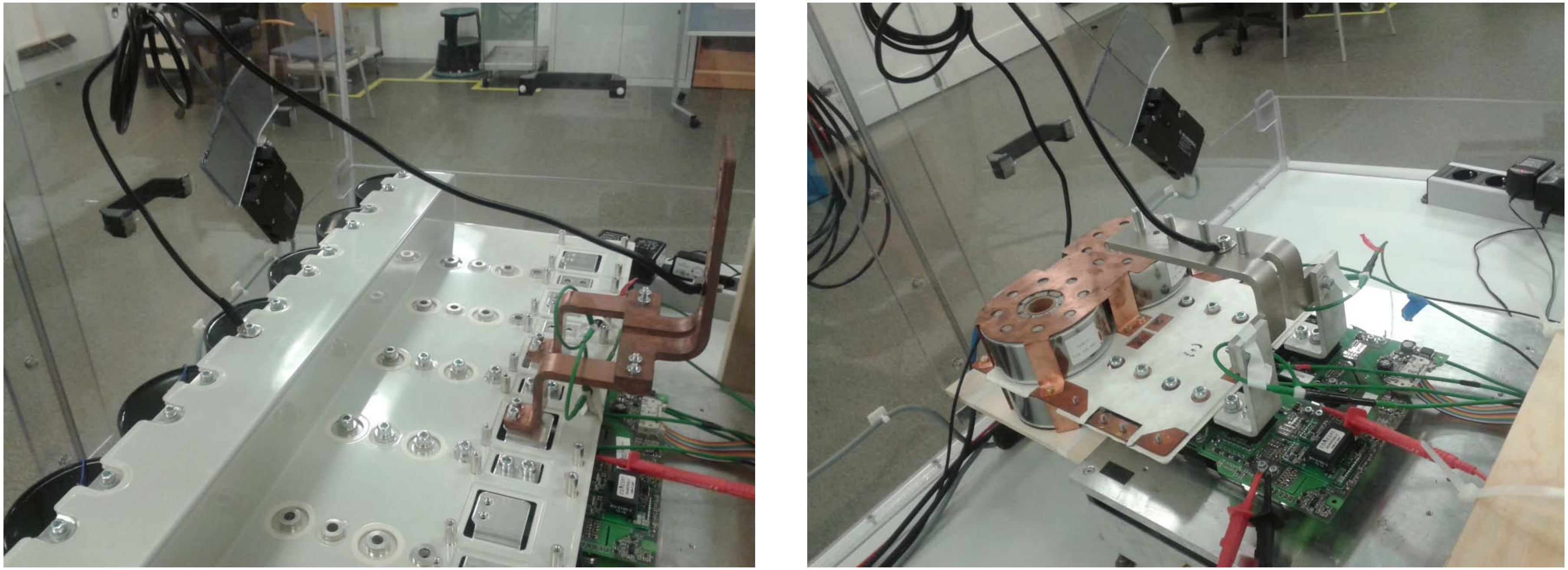
SBE optimized capacitor and bus bar structure

vs

Bus bar from Danfoss power stack equipped with an already low stray inductance film can style capacitor bank

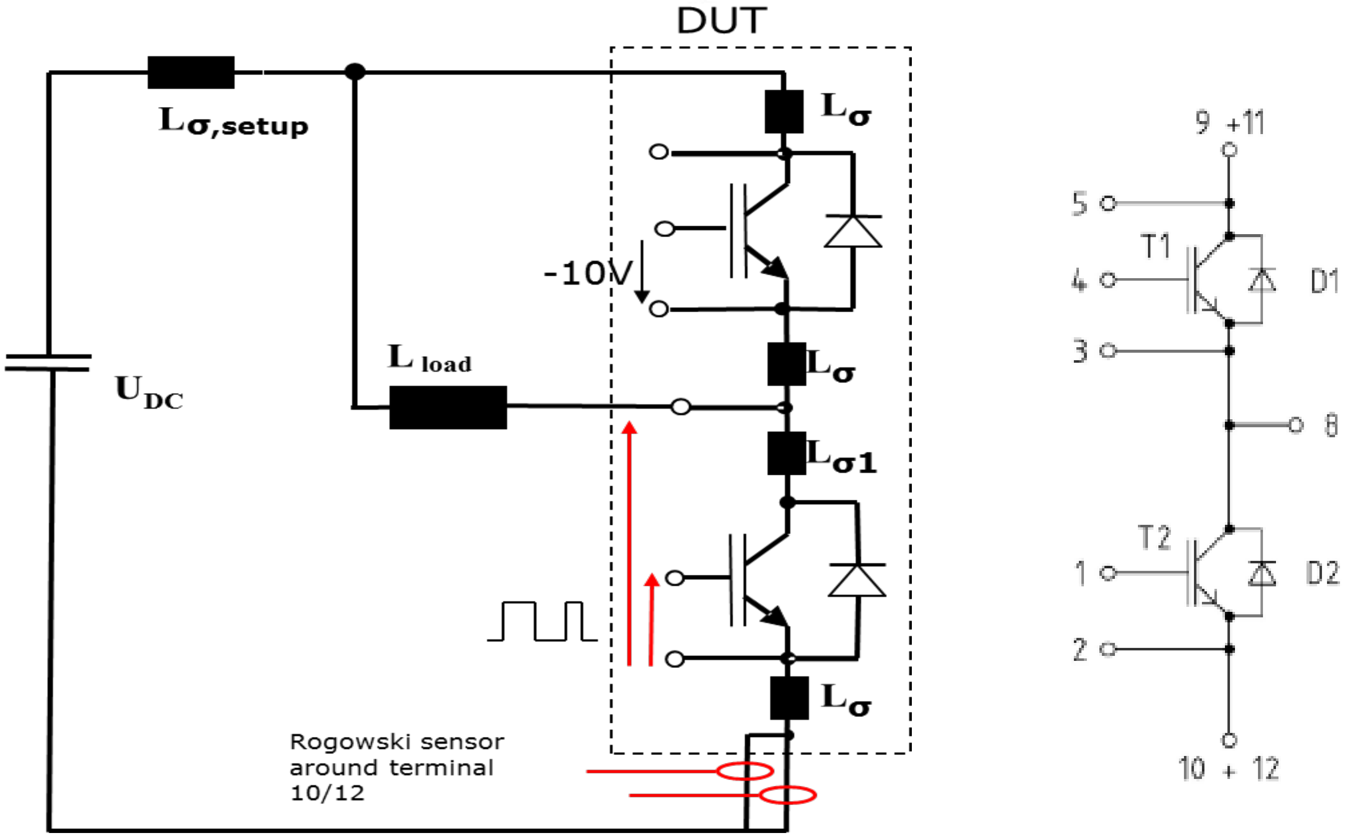
Double pulse test applied to measure overvoltage during turn-off and di/dt and ΔV during turn-on to calculate the stray inductance for both cases.

Testing at Danfoss Silicon Power (2)



Bus bar with capacitors: left: Danfoss, right SBE Power Ring Capacitors

Testing at Danfoss Silicon Power (3)



Schematic of the test setup and probe placement

Testing at Danfoss Silicon Power (4)

- Measurements taken at lower transistor while upper IGBT is kept in the off condition,
- Base plate temperature of module under test maintained at 25C,
- Differential voltage probes connected between terminals 1-2 & terminals 3-2,
- Rogowski Current Transducers placed around module terminals 10 & 12.

Testing at Danfoss Silicon Power (5)

Total *stray inductance calculated by measuring di/dt and the DC-link voltage dip at the AUX terminals at IGBT module at turn on:* $L_s = \Delta V \times di/dt$

Standard capacitor bus bar	SBE optimized module bus bar
DC-link voltage: 1100V Peak current during turn on: 1200A	
ΔU = 296 V dI/dt = 12.3 kA/µS	ΔU = 224 V dI/dt = 14.7 kA/µS
L_s = 24 nH	**L_s = 15 nH**

Testing at Danfoss Silicon Power (6)

Partial *stray inductance calculated by measuring di/dt and the voltage* V_{ce} *across the whole module, does not take into account the IGBTs internal inductance*

SBE optimized module bus bar	
ΔU = 65 V dI/dt = 14.7 kA/µS	
Stray inductance of capacitors & bus bar only	**Stray inductance of IGBT modules only**
L_s = 4.4 nH	**L_{IGBTs} ~ 10 nH**

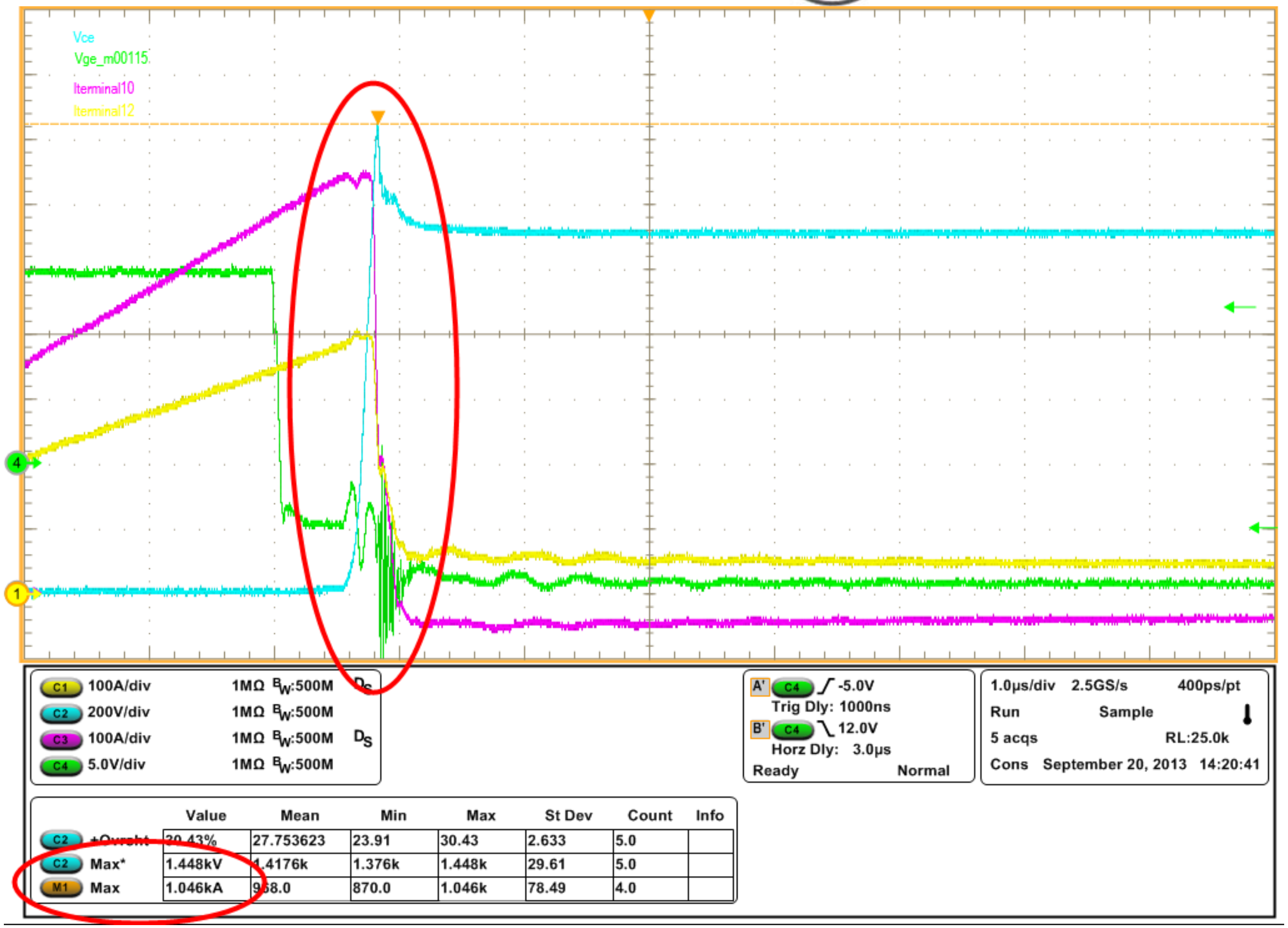
Results compatible with datasheet claims

Testing at Danfoss Silicon Power (7)

*Voltage measurements at turn off, show **20% less overshoot** when using SBE Power Ring optimized DC Link bus bar*

Standard capacitor bus bar	SBE optimized module bus bar
DC-link voltage: 1100V	
ΔU = 448 V Peak current during turn off = 1000 A	**ΔU = 348 V** Peak current during turn off = 1046 A
20% less overshoot using SBE Power Ring technology	

Testing at Danfoss Silicon Power (8)



C1 100A/div 1MΩ B_W:500M D_S
C2 200V/div 1MΩ B_W:500M
C3 100A/div 1MΩ B_W:500M D_S
C4 5.0V/div 1MΩ B_W:500M

A' C4 ╱ -5.0V
Trig Dly: 1000ns
B' C4 ╲ 12.0V
Horz Dly: 3.0µs
Ready Normal

1.0µs/div 2.5GS/s 400ps/pt
Run Sample
5 acqs RL:25.0k
Cons September 20, 2013 14:20:41

	Value	Mean	Min	Max	St Dev	Count	Info
C2 +Ovrsht	30.43%	27.753623	23.91	30.43	2.633	5.0	
C2 Max*	1.448kV	1.4176k	1.376k	1.448k	29.61	5.0	
M1 Max	1.046kA	968.0	870.0	1.046k	78.49	4.0	

Example of SBE module turn off oscilloscopic measurement:

Purple curve = total current

Blue curve = voltage at IGBT terminals

Conclusions (1)

Optimized DC link capacitor/bus configuration with ESL < 5nH (magneto-dynamic analysis, ring-out & overshoot measurement validation)

⇩

Reduction in overshoot voltage of more than 20%

⇩

20% increase in inverter power achieved with the same investment in silicon

⇩

Advantage in the highly competitive alternative energy market space.

Questions

Thank you