Low Inductance – Low Temp Rise DC Bus Capacitor Properties Enabling the Optimization of High Power Inverters

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Overview

- Methods of determining low ESL capacitor measurements accurately
  - ESL can then be applied to switch design simulation tools to optimize inverter
- Optimizing efficiency of high power inverter with low temperature rise
- System design advantages to measure ESR and impact on temperature rise
- Discussing example of customer using drive cycle power information applied to capacitor temperature rise simulation information

DC Link Capacitor ESL Measurements

- Test method to determine total inductance from DC link capacitor windings to the switch device terminals
- Charge the capacitor at low voltage and discharge
  - Observe the voltage waveform on the discharge ring-out
- Loop inductance and capacitance can be obtained through simple circuit element calculations

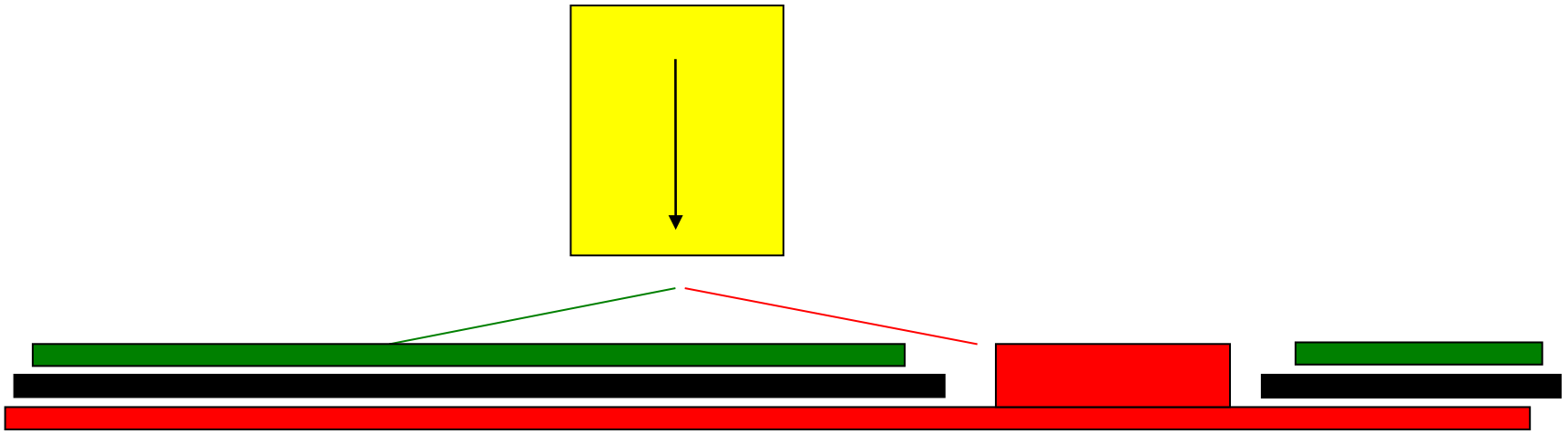
DC Link Capacitor ESL Measurements

Bus short circuit device attributes for accuracy

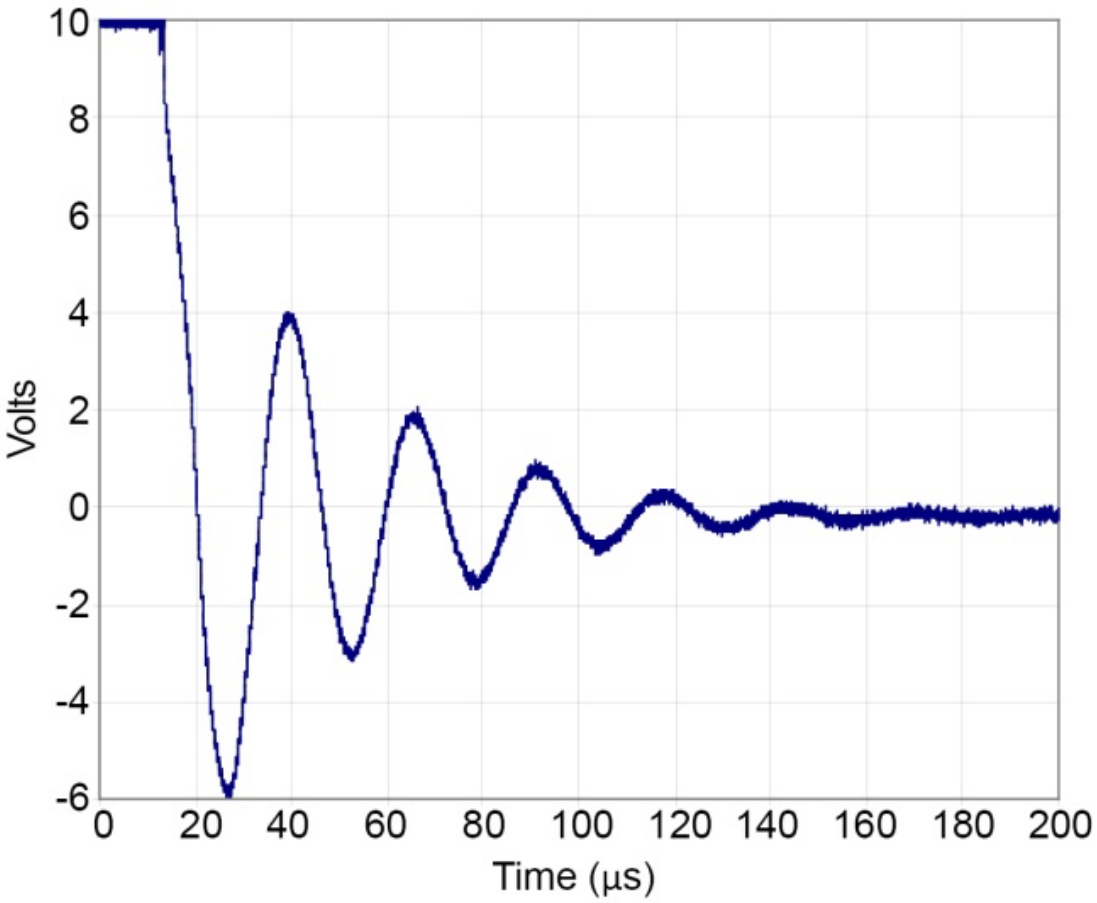
- Minimal added inductance
- No contact bounce
- Fast closure
- Very low contact resistance
- Relatively long life
- Repeatable “on resistance”

DC Link Capacitor ESL Measurements

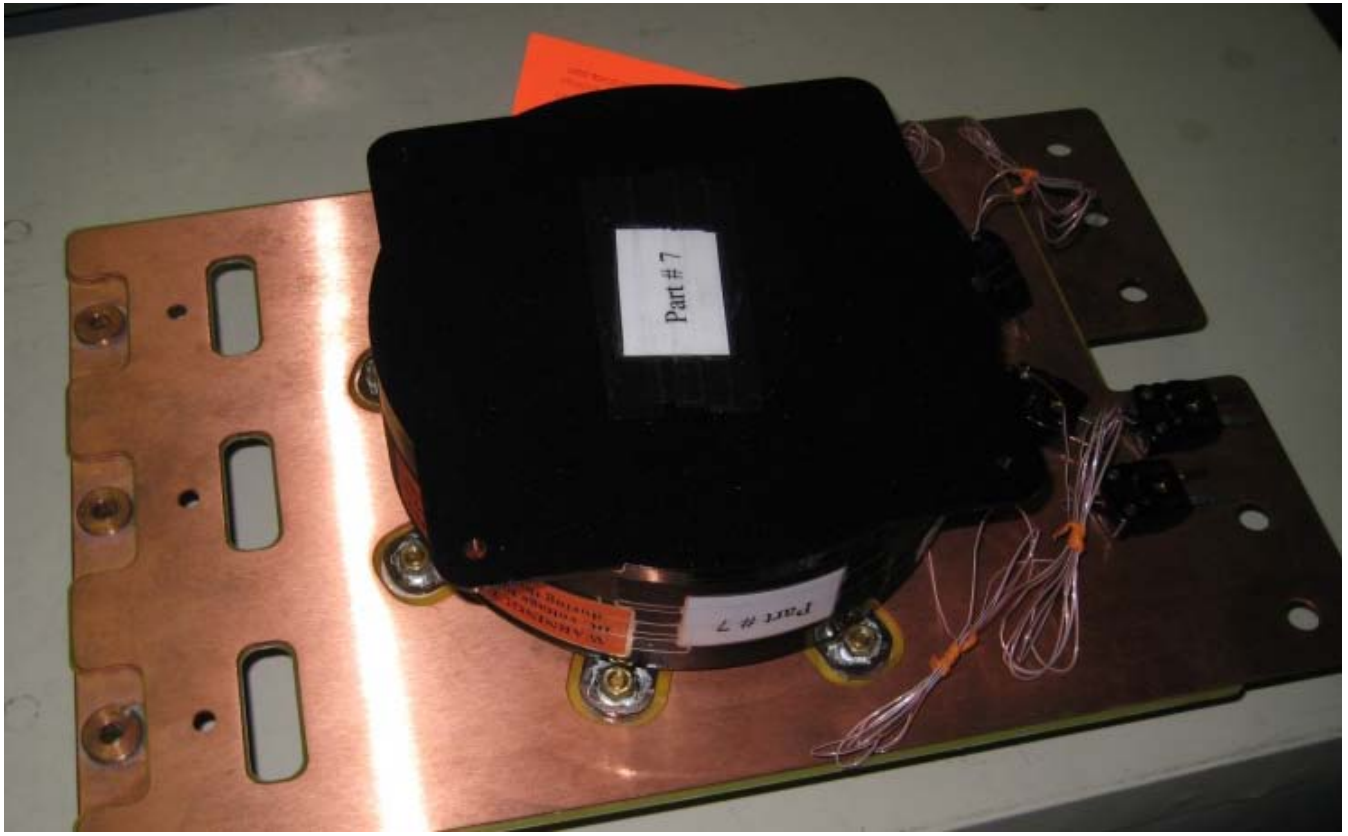
- Concept diagram for the DC link capacitor shorting device (Black is insulator, Red and Green are +/- of bus)



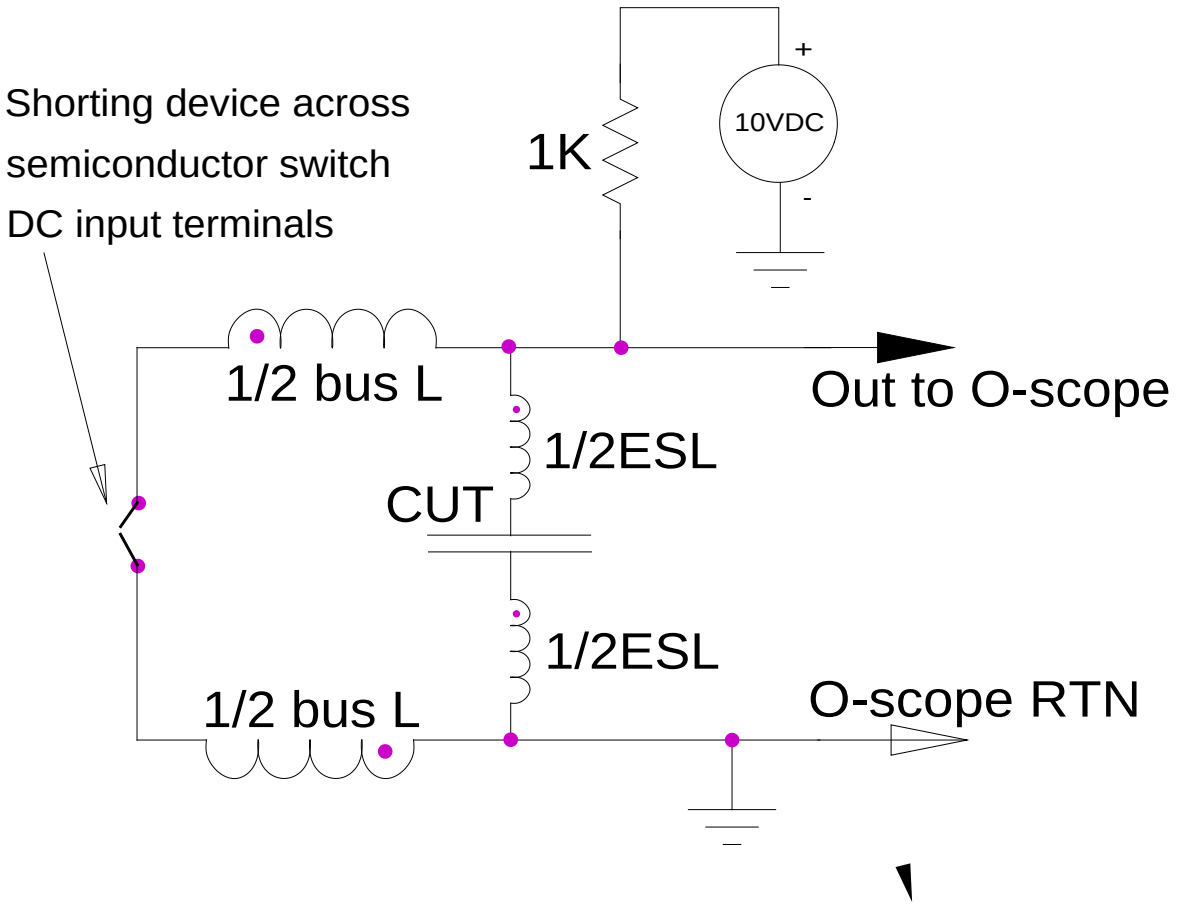
DC Link Capacitor ESL Measurements



SBE Power Ring with Coplanar Bus



Equivalent Circuit of the Shorting Test Assembly



Inductance and ESL

- $L = (1/C)*(1/(2\pi f))^2$
- 2V = 10V[(Cap ESL)/(LoopL)]

- For 1000µF = C:

  f = 1/P = 1/(75µs/3) = 40khz

  L= 15.8nH

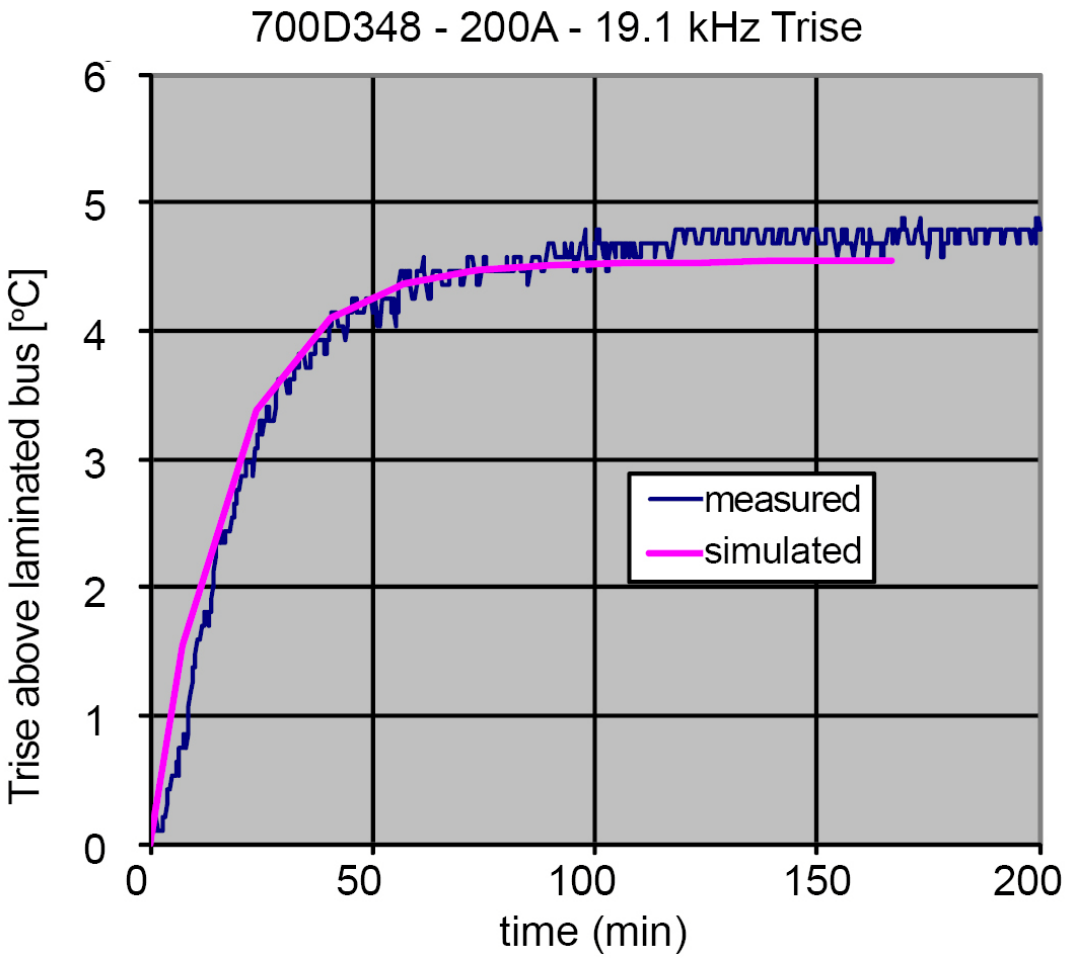
  2V = 10V [(Cap ESL)/15.8nH)

  Cap ESL = 3.2nH

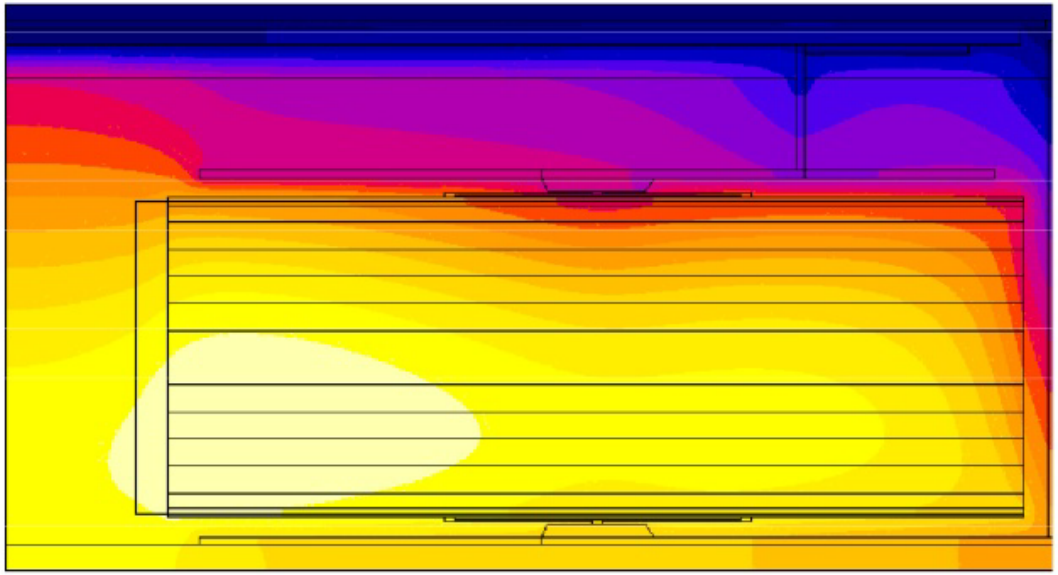
Performance Implications of Low Temperature Rise

- Design optimized to reduce bus inductance and voltage overshoot
- Annular shape provides very short path between electrodes and therefore very low ESR (0.2 – 0.5mΩ)
  - High speed winding shape is low cost to produce
  - Uses common MPP and MPE materials
- Temperature profiling tools allow for safe design migration

Measured and Simulated Trise – 1000µF



Temperature Profile – 200A – 19.1KHz



Color Shade Results (°C)

25/25.284	26.42/26.71	27.84/28.13
25.28/25.57	26.71/26.99	28.13/28.41
25.57/25.85	26.99/27.27	28.41/28.70
25.85/26.14	27.27/27.56	28.70/28.98
26.14/26.42	27.56/27.84	

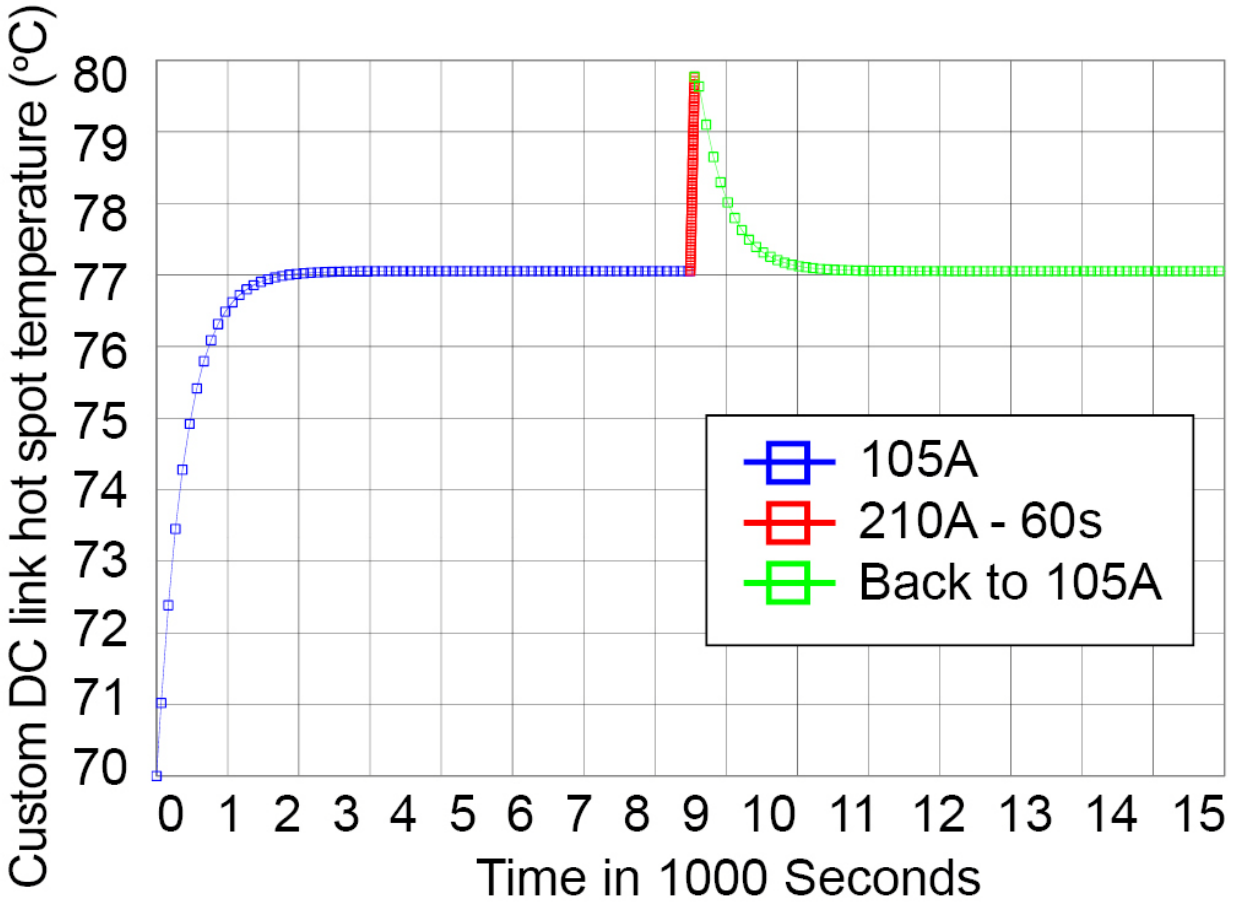
Temperature Profile

- Laminated bus heat sources:
  - AC and DC conduction sources
  - Interconnect losses
  - Thermal input from the switch semiconductor modules
  - Capacitor Thermal Losses (low contribution in this case)
- If temperature difference between laminated bus and capacitor is more than a few degrees celsius, the capacitor assembly can become a thermal path for the bus heat
  - here the capacitor hot spot will be where the terminals attach to the winding

Temperature Profile

- If capacitor used to cool the bus ,the designer needs to be aware of it, and temperature simulation will show the impact on final current rating and any reliability concerns
- Minimize bus plate temperature rise will enhance inverter reliability
- Also, preventing DC Link from becoming a thermal path with improve reliability greatly

Peak Power - Temperature Rise



Peak Power - Temperature Rise

- Electric vehicles: full load unlikely for long
  - Battery Capacity cannot handle it
- Simulation showing hot spot additional Trise of less than 3°C during 60 secs peak power
- Trise of DC Link Capacitor for any electric vehicle drive power cycle can be simulated
  - Regardless of film section shape

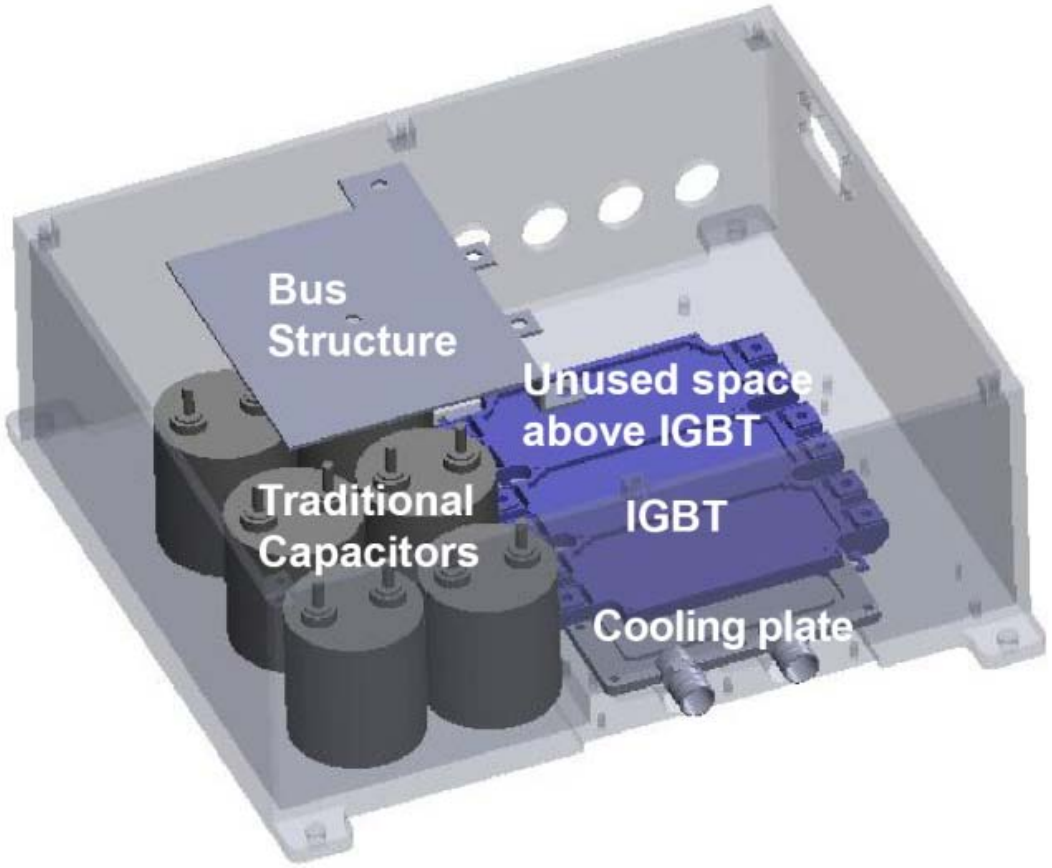
Impact of ESR/ESL on Inverter Design

Design options:

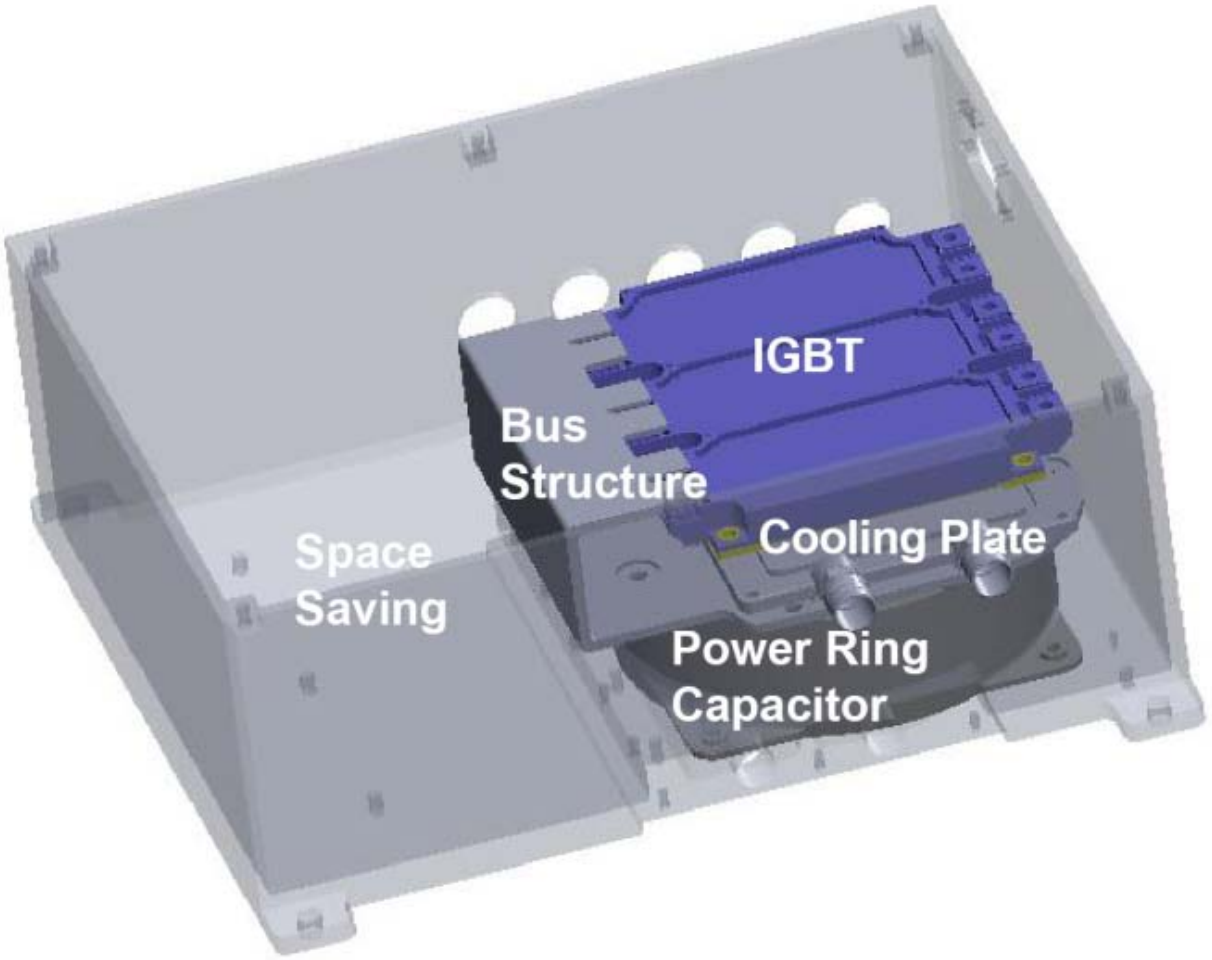
- Drop in replacement
- Modification to existing design
- Complete new design

More flexibility = more opportunity for significant impact on high density, cost, reliability and size

Typical Planer Inverter Layout

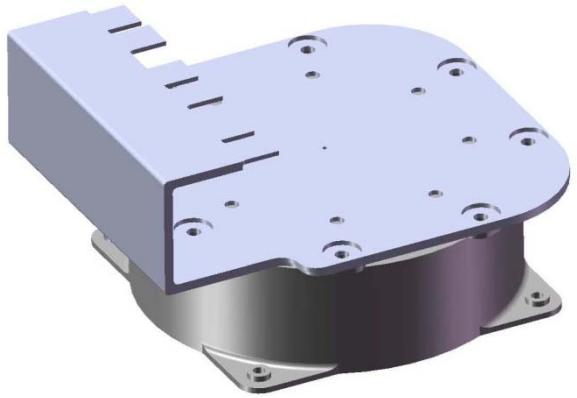


Stacked Vertical IGBT with Power Ring



Stacked Vertical IGBT with Power Ring

- Design
  - Short, equal length connections
  - High current handling
  - Direct interface of both IGBTs and DC Link Capacitor to heat sink
- Simulation Tools to validate thermal assumptions and predict reliability



Stacked Vertical IGBT with Power Ring

- Results
  - Tighter, more compact inverter
  - Significantly reduced voltage overshoot and switching losses
  - 30% volume reduction
  - Higher reliability without increased cost